DATA SHEET

74AC125/74ACT125
Quad buffer/line driver (3-state)

Product specification

1997 May 15

Philips
Semiconductors

PHILIPS

Quad buffer/line driver (3-state)

74AC125
74ACT125

FEATURES

- 74ACT125 has TTL-compatible inputs
- 74AC125 has CMOS-compatible inputs
- 3-State outputs source/sink 24mA
- 3-State outputs drive bus lines or buffer memory address registers
- Meets or exceeds JEDEC standard standard for 74AC(T)XX family

DESCRIPTION

The 74AC125/74ACT125 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74AC125/74ACT125 consists of four independent non-inverting buffers/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the associated output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL			UNIT
			AC		ACT	
			V_{CC} = 3.3V	V_{CC} = 5.0V	V_{CC} = 5.0V	
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 50pF V_{CC} = 3.3V	3.4	2.4	3.8	ns
C_I	Input capacitance		4.5			pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1] outputs enabled outputs disabled	22 5		18 3	pF

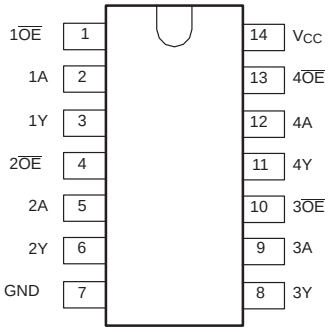
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
14-Pin Plastic SOL	–40°C to +85°C	74AC125D 74ACT125D	74AC125D 74ACT125D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74AC125DB 74ACT125DB	74AC125DB 74ACT125DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74AC125PW 74ACT125PW	74AC125PW DH 74ACT125PW DH	SOT402-1

PIN CONFIGURATION



SV00455

PIN DESCRIPTION

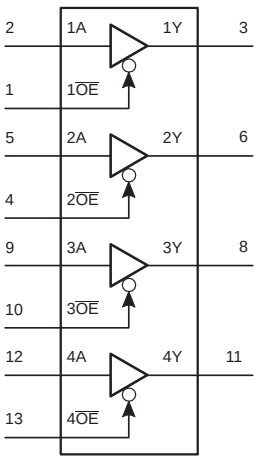
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1$\overline{OE}$ to 4$\overline{OE}$	Data enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	Data inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
n$\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL



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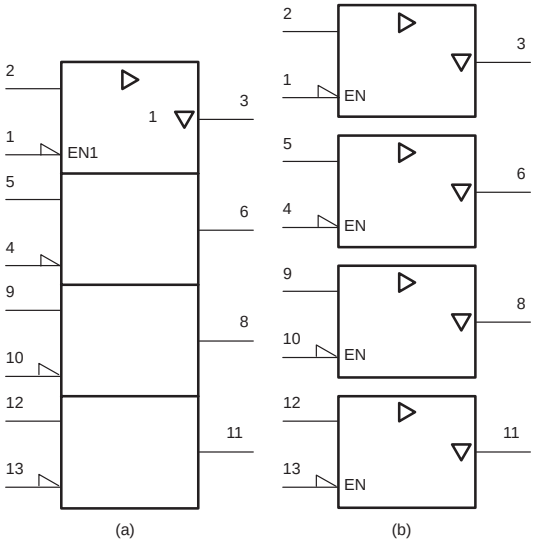
LOGIC SYMBOL (IEEE/IEC)



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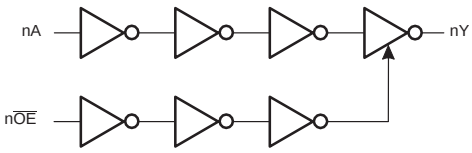
LOGIC DIAGRAM



SV00789

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage for 'AC	2.0	6.0	V
V_{CC}	DC supply voltage for 'ACT	4.5	5.5	V
V_{IN}	DC input voltage range	0	V_{CC}	V
V_O	DC output voltage range	0	V_{CC}	V
T_{amb}	Operating free-air temperature range	–40	+85	°C
$\Delta V/\Delta t$	Minimum input edge rate — AC devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125		mV/ns
	— ACT devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125		

ABSOLUTE MAXIMUM RATINGS[1]

in accordance with the Absolute Maximum Rating System (IEC134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	V_{IN} = –0.5V	–20	mA
		V_{IN} = V_{CC} + 0.5V	+20	
V_{IN}	DC input voltage		–0.5 to V_{CC} +0.5	V
I_{OK}	DC output diode current	V_O = –0.5V	–20	mA
		V_O = V_{CC} + 0.5V	+20	
V_O	DC output voltage		–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current		± 50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current per output		± 50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current		± 200	mA
T_{stg}	Storage temperature range		–65 to 150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (74AC125)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	3.0	2.1	1.5		V
			4.5	3.15	2.25		
			5.5	3.85	2.75		
V_{IL}	LOW level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	3.0		1.5	0.9	V
			4.5		2.25	1.35	
			5.5		2.75	1.65	
V_{OH}	HIGH level output voltage	I_{OUT} = –50 μA	3.0	2.9	2.99		V
			4.5	4.4	4.49		
			5.5	5.4	5.49		
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –12mA[1]	3.0	2.46			V
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	4.5	3.76			
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	5.5	4.76			
V_{OL}	LOW level output voltage	I_{OUT} = 50 μA	3.0		0.01	0.1	V
			4.5		0.01	0.1	
			5.5		0.01	0.1	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 12mA[1]	3.0			0.44	V
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	4.5			0.44	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	5.5			0.44	
I_{IN}	Input leakage current	V_{IN} = V_{CC}, GND	5.5			±1.0	μA
I_{OZ}	3-State output OFF-state current	V_{IN} (OE) = V_{IL}, V_{IH} V_{IN} = V_{CC}, GND V_{OUT} = V_{CC}, GND	5.5			±2.5	μA
I_{OLD}[2]	Dynamic output current[2]	V_{OLD} = 1.65V max	5.5	75			mA
I_{OHD}[2]	Dynamic output current[2]	V_{OHD} = 3.85V min	5.5			–75	mA
I_{CC}	Quiescent supply current	V_{IN} = V_{CC} or GND	5.5			40	μA

NOTES:
1. All outputs loaded
2. Maximum test duration 2.0 ms; one output loaded at a time

DC ELECTRICAL CHARACTERISTICS (74ACT125)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	4.5	2.0	1.5		V
			5.5	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	4.5		1.5	0.8	V
			5.5		1.5	0.8	
V_{OH}	HIGH level output voltage	I_{OUT} = –50 μA	4.5	4.4	4.49		V
			5.5	5.4	5.49		
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	4.5	3.76			V
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	5.5	4.76			
V_{OL}	LOW level output voltage	I_{OUT} = 50 μA	4.5		0.01	0.1	V
			5.5		0.01	0.1	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	4.5			0.44	V
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	5.5			0.44	
I_{IN}	Input leakage current	V_{IN} = V_{CC}, GND	5.5			±1.0	μA
I_{OZ}	3-State output OFF-state current	V_{IN} (OE) = V_{IL}, V_{IH} V_{IN} = V_{CC}, GND V_{OUT} = V_{CC}, GND	5.5			±2.5	μA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{IN} = V_{CC} – 2.1V Other inputs at V_{CC} or GND; I_{OUT} = 0	5.5			1.5	mA
I_{OLD}[2]	Dynamic output current	V_{OLD} = 1.65V max	5.5	75			mA
I_{OHD}[2]	Dynamic output current	V_{OHD} = 3.85V min	5.5			–75	mA
I_{CC}	Quiescent supply current	V_{IN} = V_{CC} or GND	5.5			40	μA

NOTES:
1. All outputs loaded
2. Maximum test duration 2.0ms, one output loaded at a time

AC CHARACTERISTICS FOR 74AC125

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω; .

SYMBOL	PARAMETER	V_{CC}[1] (V)	LIMITS					UNIT	WAVEFORM
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay nA to nY	3.3 5.0	2.0 1.5	3.4 2.4	9.0 6	1.5 1.0	10 7	ns	1, 3
t_{PHL}	Propagation delay nA to nY	3.3 5.0	2.0 1.5	3.4 2.5	9.0 6	1.5 1.0	10 7	ns	1, 3
t_{PZH}	3-State output enable time $n\overline{OE}$ to nY	3.3 5.0	2.0 1.5	4.3 2.9	9.5 6.5	1.5 1.0	11 7.5	ns	2, 3
t_{PZL}	3-State output enable time $n\overline{OE}$ to nY	3.3 5.0	2.0 1.5	4.7 3.2	9.5 6.5	1.5 1.0	11 7.5	ns	2, 3
t_{PHZ}	3-State output disable time $n\overline{OE}$ to nY	3.3 5.0	2.0 1.5	4.4 2.9	9.0 6	1.5 1.0	10 7	ns	2, 3
t_{PLZ}	3-State output disable time $n\overline{OE}$ to nY	3.3 5.0	2.0 1.5	4.2 3.0	9.0 6	1.5 1.0	10 7	ns	2, 3

NOTE:

1. Voltage range 3.3V is V_{CC} = 3.3V ± 0.3V
   Voltage range 5.0V is V_{CC} = 5.0V ± 0.5V

AC CHARACTERISTICS FOR 74ACT125

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω; .

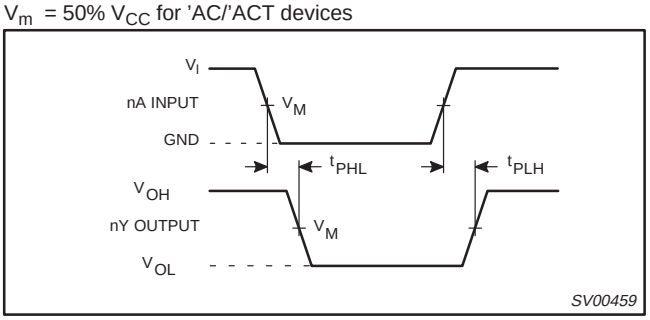
SYMBOL	PARAMETER	V_{CC}[1] (V)	LIMITS					UNIT	WAVEFORM
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay nA to nY	5.0	2.0	4.4	9.0	1.5	10	ns	1, 3
t_{PHL}	Propagation delay nA to nY	5.0	2.0	3.3	9.0	1.5	10	ns	1, 3
t_{PZH}	3-State output enable time $n\overline{OE}$ to nY	5.0	2.0	3.7	8.5	1.5	9.5	ns	2, 3
t_{PZL}	3-State output enable time $n\overline{OE}$ to nY	5.0	2.0	4	8.5	1.5	9.5	ns	2, 3
t_{PHZ}	3-State output disable time $n\overline{OE}$ to nY	5.0	2.0	4	8.0	1.5	9	ns	2, 3
t_{PLZ}	3-State output disable time $n\overline{OE}$ to nY	5.0	2.0	3.8	8.0	1.5	9	ns	2, 3

NOTE:

1. Voltage range 5.0V is V_{CC} = 5.0V ± 0.5V

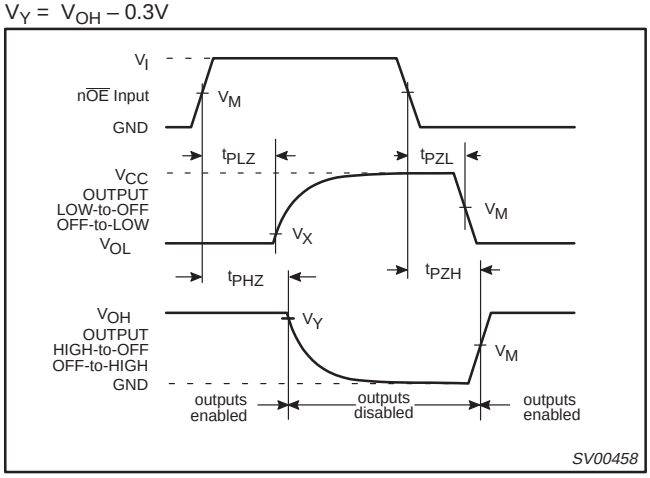
AC WAVEFORMS

V_m = 50% V_{CC} for 'AC devices; 1.5V for 'ACT devices
V_m = 50% V_{CC} for 'AC/'ACT devices



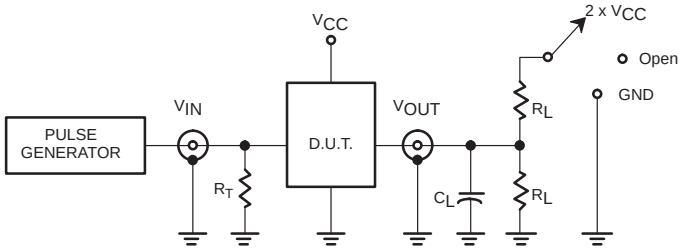
Waveform 1. Input (nA) to output (nY) propagation delays and output transition times.

V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load.
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$



Waveform 2. 3-state enable and disable times.

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	Open

FAMILY	V_{IN} Input Requirements	V_m Input	V_m Output
AC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
ACT	GND to 3.0V	1.5V	50% V_{CC}

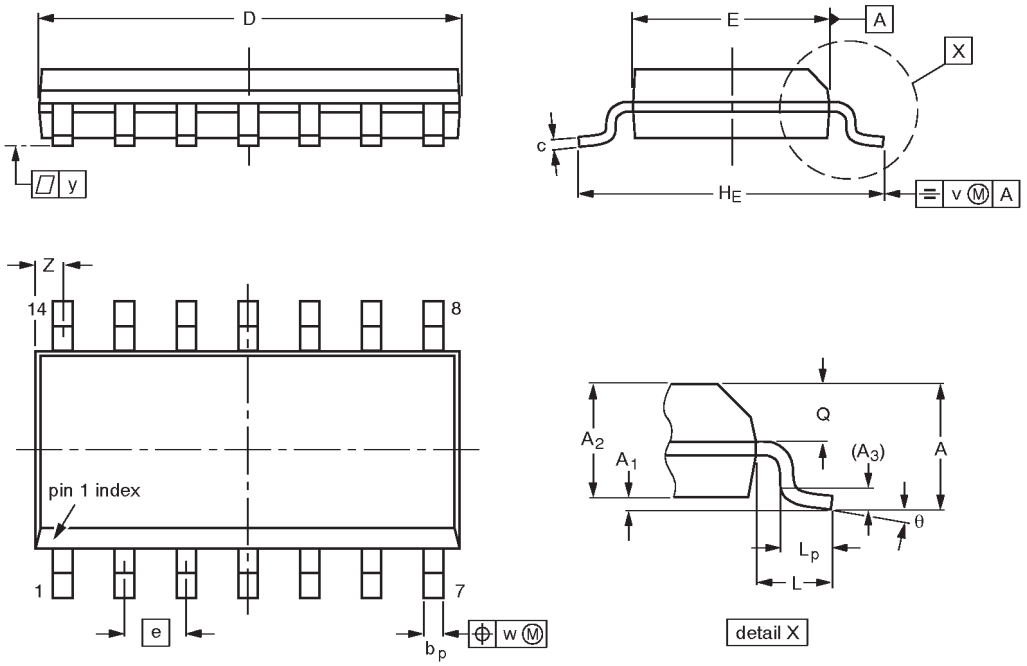
DEFINITIONS

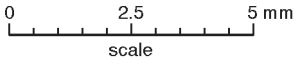
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance, see AC characteristics
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SV00451

Waveform 3. Load circuitry for switching times.

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

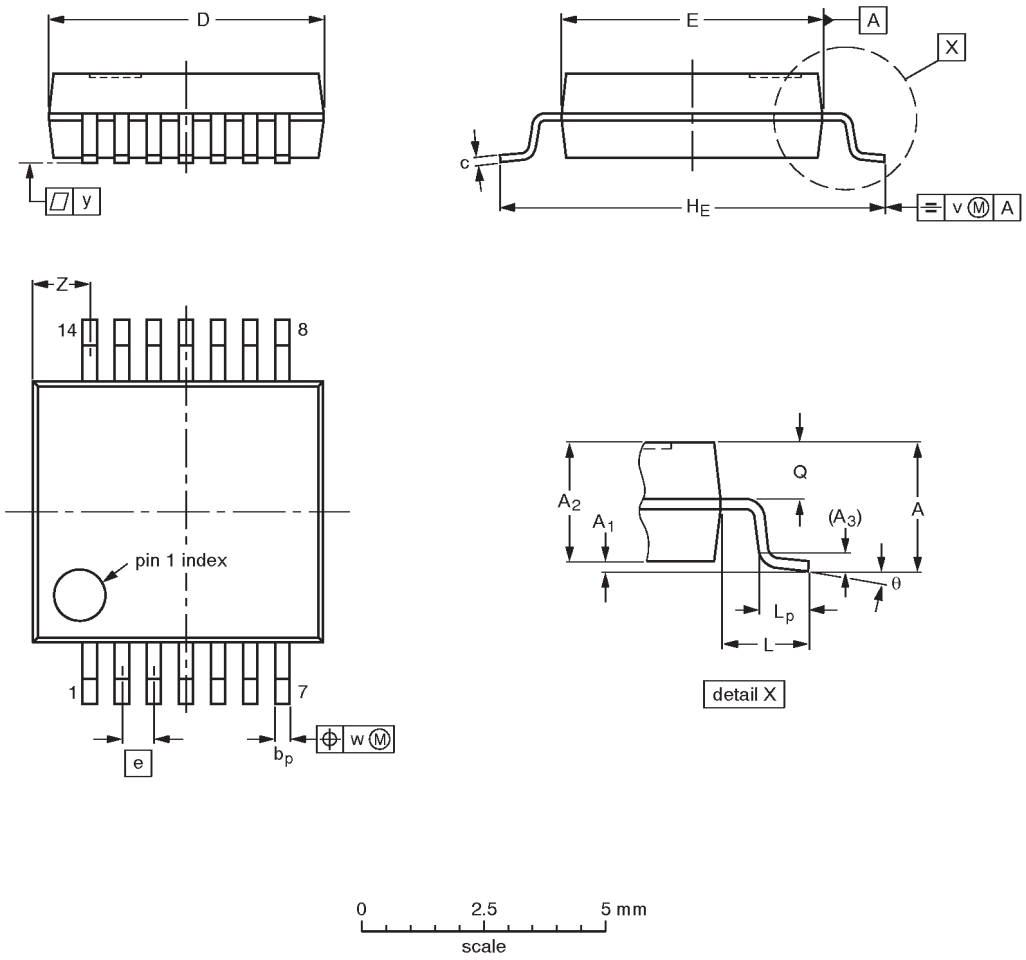
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~91-08-13~~ 95-01-23

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

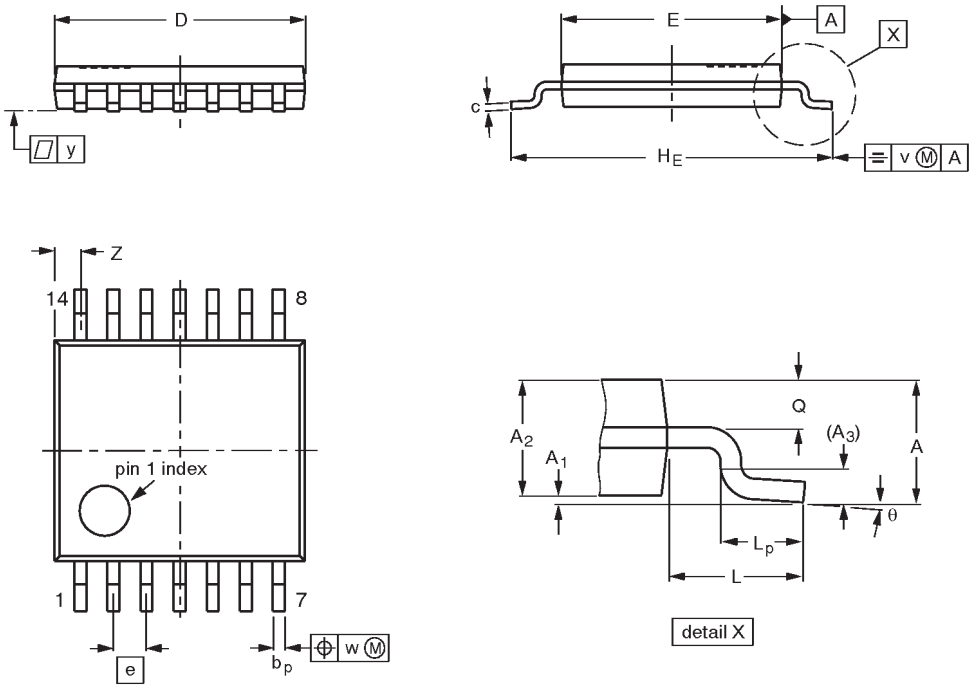
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

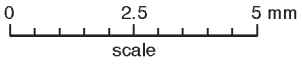
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				~~95-02-04~~ 96-01-18

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~94-07-12~~ 95-04-04

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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