

## Fast CMOS Octal Transparent Latches

### Product Features:

- PI74FCT373/533/573T have the same speed and drive of Bipolar FAST™ "F" series, at CMOS power levels.
  - "A" speeds at 5.2 ns max.
  - "C" speeds at 4.2 ns max.
  - "D" speeds are an industry first, at 3.8 ns max.
- TTL input and output levels, reducing problematic "ground bounce"
- High output drive,  $I_{OL} = 64$  mA
- Extremely low static power (1 mW, typ.)
- Industry standard pinout, plug into existing "74F" sockets for speed enhancement at reduced power levels
- Octal transparent latch with 3-state output control
- Hysteresis on all inputs
- Packaged in 20-pin plastic DIP, surface mount SOIC, or the industry's new "1/4 size" surface mount QSOP

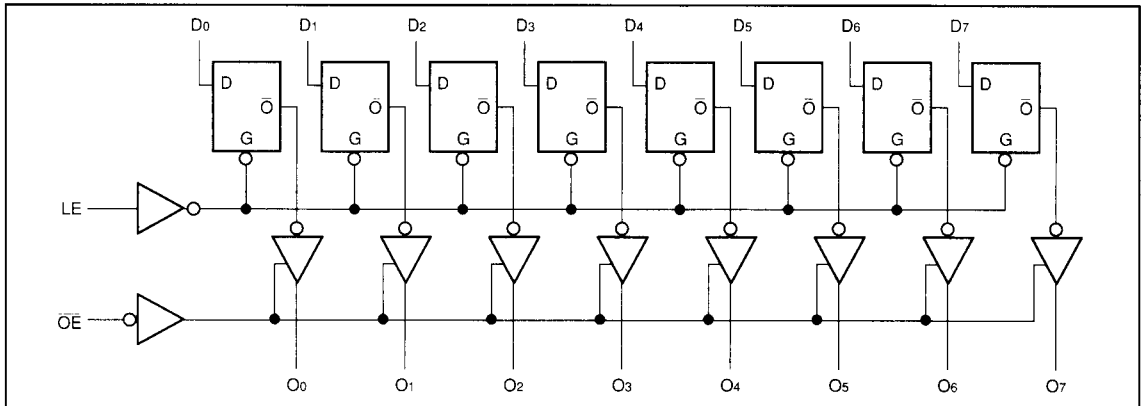
### Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

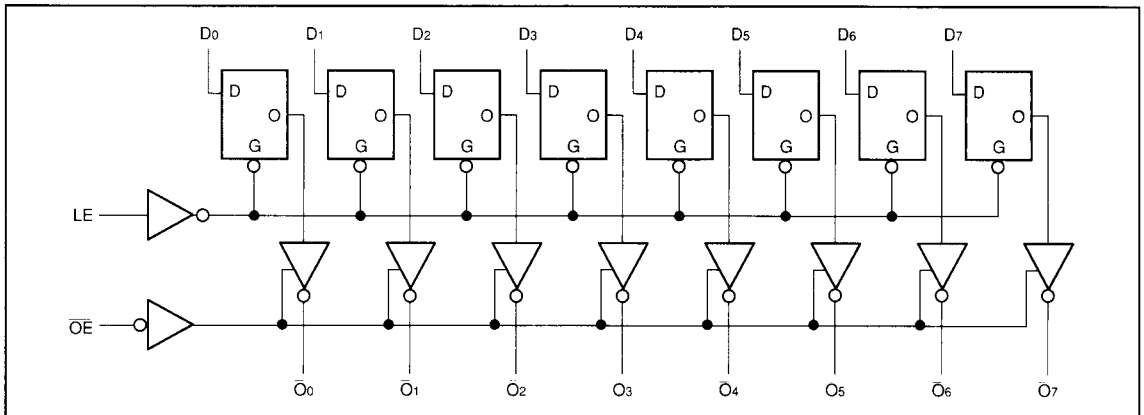
The PI74FCT373T, 533T, and 573T are 8-bit wide octal transparent latches designed with 3-state outputs and are intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When  $\overline{OE}$  is HIGH, the bus output is in the high impedance state.

All products are available in three package types: 20-pin, 300 mil wide plastic DIP, 300 mil wide plastic SOIC, and the industry's new 150 mil wide QSOP (one quarter the size of an SOIC).

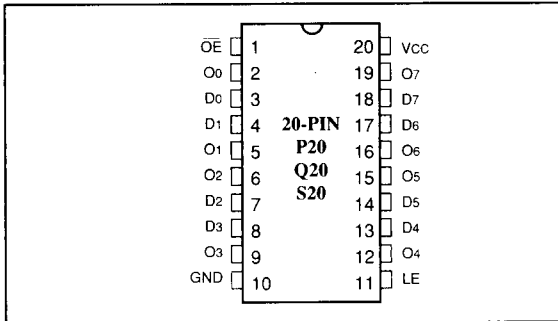
### PI74FCT373T and PI74FCT573T Logic Block Diagram



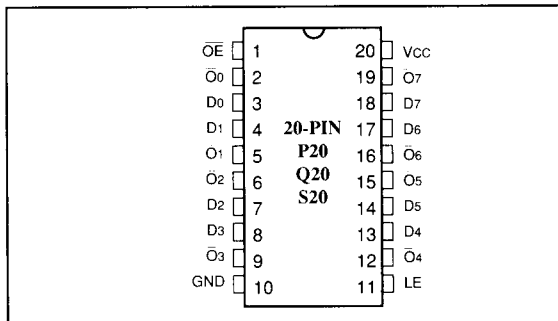
### PI74FCT533T Logic Block Diagram



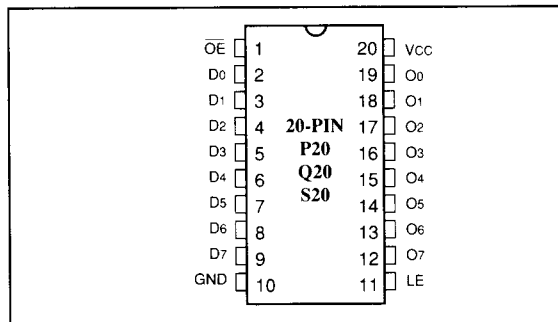
### PI74FCT373T Product Pin Configuration



### PI74FCT533T Product Pin Configuration



### PI74FCT573T Product Pin Configuration



### Product Pin Description

Pin Name	Description
OE	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D0-D7	Data Inputs
O0-O7	3-State Outputs
00-07	Complementary 3-State Outputs
GND	Ground
Vcc	Power

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### PI74FCT533T Truth Table<sup>(1)</sup>

D <sub>N</sub>	Inputs		Outputs
	LE	OE	O <sub>N</sub>
H	H	L	L
L	H	L	H
X	X	H	Z

### PI74FCT373/573T Truth Table<sup>(1)</sup>

D <sub>N</sub>	Inputs		Outputs
	LE	OE	O <sub>N</sub>
H	H	L	H
L	H	L	L
X	X	H	Z

- H = High Voltage Level  
L = Low Voltage Level  
X = Don't Care  
Z = High Impedance

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only) .....	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) .....	-0.5V to Vcc
DC Input Voltage .....	-0.5V to +7.0V
DC Output Current .....	120 mA
Power Dissipation .....	0.5W

**Note:**

Stresses greater than those listed under **MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC Electrical Characteristics** (Over the Operating Range,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ )

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ <sup>(2)</sup>	Max.	Units	
VOH	Output HIGH Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8.0 \text{ mA}$	2.4	3.3		V
			$I_{OH} = -15.0 \text{ mA}$	2.0	3.0		V
VOL	Output LOW Current	$V_{CC} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$		0.3	0.55	V	
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V	
VIL	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V	
IiH	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = 2.7 \text{ V}$			5	$\mu\text{A}$	
IiL	Input LOW Current	$V_{CC} = \text{Max.}, V_{IN} = 0.5 \text{ V}$			-5	$\mu\text{A}$	
IOZH	High Impedance	$V_{CC} = \text{Max.}, V_{OUT} = 2.7 \text{ V}$			+10	$\mu\text{A}$	
IOZL	Output Current	$V_{CC} = \text{Max.}, V_{OUT} = 0.5 \text{ V}$			-10	$\mu\text{A}$	
Ii	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC} (\text{Max.})$			20	$\mu\text{A}$	
Vik	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V	
Ios	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_{OUT} = \text{GND}$	-60	-120		mA	
IOFF	Power Down Disable	$V_{CC} = \text{GND.}, V_{OUT} = 4.5 \text{ V}$	—	—	100	$\mu\text{A}$	
VH	Input Hysteresis			200		mV	

**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $f = 1 \text{ MHz}$ )

Parameters <sup>(4)</sup>	Description	Test Conditions	Typ	Max.	Units
CIN	Input Capacitance	$V_{IN} = 0 \text{ V}$	6	10	pF
COU	Output Capacitance	$V_{OUT} = 0 \text{ V}$	8	12	pF

**Notes:**

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0$ ,  $+25^\circ\text{C}$  ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

**Power Supply Characteristics**

Parameters	Description	Test Conditions <sup>(1)</sup>		Min.	Typ <sup>(2)</sup>	Max.	Units
I <sub>cc</sub>	Quiescent Power Supply Current	V <sub>cc</sub> = Max.	V <sub>IN</sub> = GND or V <sub>cc</sub>		0.2	1.5	mA
ΔI <sub>cc</sub>	Supply Current per Input @ TTL HIGH	V <sub>cc</sub> = Max.,	V <sub>IN</sub> = 3.4 V <sup>(3)</sup>		0.5	2.5	mA
I <sub>ccd</sub>	Supply Current per Input per MHz <sup>(4)</sup>	V <sub>cc</sub> = Max., Outputs Open OE = GND LE = V <sub>cc</sub> One Bit Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>cc</sub> V <sub>IN</sub> = GND		0.15	0.25	mA/ MHz
I <sub>c</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>cc</sub> = Max., Outputs Open f <sub>i</sub> = 10 MHz 50% Duty Cycle OE = GND LE = V <sub>cc</sub> One Bit Toggling	V <sub>IN</sub> = V <sub>cc</sub> V <sub>IN</sub> = GND		1.7	4.0 <sup>(5)</sup>	mA
			V <sub>IN</sub> = 3.4 V V <sub>IN</sub> = GND		2.0	5.0 <sup>(5)</sup>	
		V <sub>cc</sub> = Max., Outputs Open f <sub>i</sub> = 2.5 MHz 50% Duty Cycle OE = GND LE = V <sub>cc</sub> Eight Bits Toggling	V <sub>IN</sub> = V <sub>cc</sub> V <sub>IN</sub> = GND		3.2	6.5 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4 V V <sub>IN</sub> = GND		5.2	14.5 <sup>(5)</sup>	

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**Notes:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V<sub>cc</sub> = 5.0 V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>cc</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>cc</sub> formula. These limits are guaranteed but not tested.
- I<sub>c</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_c = I_{cc} + \Delta I_{cc} D_H N_T + I_{ccd} (f_{CP}/2 + f_i N_i)$   
 I<sub>cc</sub> = Quiescent Current  
 ΔI<sub>cc</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4 V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>ccd</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

**PI74FCT373T Switching Characteristics over Operating Range**

Parameters	Description	Conditions <sup>(1)</sup>	FCT373T		FCT373AT		FCT373CT		FCT373DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	ns
t <sub>PHL</sub>	D <sub>N</sub> to O <sub>N</sub>										
t <sub>PLH</sub>	Propagation Delay		2.0	13.0	2.0	8.5	2.0	5.5	2.0	4.0	ns
t <sub>PHL</sub>	LE to O <sub>N</sub>										
t <sub>PZH</sub>	Output Enable Time		1.5	12.0	1.5	6.5	1.5	5.5	1.5	4.8	ns
t <sub>PZL</sub>											
t <sub>PHZ</sub>	Output Disable Time		1.5	7.5	1.5	5.5	1.5	5.0	1.5	4.0	ns
t <sub>PLZ</sub>											
t <sub>SU</sub>	Set-up Time HIGH or LOW, D <sub>N</sub> to LE		2.0	—	2.0	—	2.0	—	1.5	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW, D <sub>N</sub> to LE		1.5	—	1.5	—	1.5	—	1.0	—	ns
t <sub>W</sub>	LE Pulse Width HIGH	6.0	—	5.0	—	5.0	—	3.0	—	ns	

**PI74FCT533T Switching Characteristics over Operating Range**

Parameters	Description	Conditions <sup>(1)</sup>	FCT533T		FCT533AT		FCT533CT		FCT533DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	1.5	10.0	1.5	5.2	1.5	4.2	1.5	3.8	ns
t <sub>PHL</sub>	D <sub>N</sub> to O <sub>N</sub>										
t <sub>PLH</sub>	Propagation Delay		2.0	13.0	2.0	8.5	2.0	5.5	2.0	4.0	ns
t <sub>PHL</sub>	LE to O <sub>N</sub>										
t <sub>PZH</sub>	Output Enable Time		1.5	11.0	1.5	6.5	1.5	5.5	1.5	4.8	ns
t <sub>PZL</sub>											
t <sub>PHZ</sub>	Output Disable Time		1.5	7.0	1.5	5.5	1.5	5.0	1.5	4.0	ns
t <sub>PLZ</sub>											
t <sub>SU</sub>	Set-up Time HIGH or LOW, D <sub>N</sub> to LE		2.0	—	2.0	—	2.0	—	1.5	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW, D <sub>N</sub> to LE		1.5	—	1.5	—	1.5	—	1.0	—	ns
t <sub>W</sub>	LE Pulse Width HIGH	6.0	—	5.0	—	5.0	—	3.0	—	ns	

**Notes:**

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

PI74FCT573T Switching Characteristics over Operating Range

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Parameters	Description	Conditions <sup>(1)</sup>	FCT573T		FCT573AT		FCT573CT		FCT573DT		Unit
			Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	ns
tPHL	DN to ON										
tPLH	Propagation Delay		2.0	12.0	2.0	8.5	2.0	5.5	2.0	4.0	ns
tPHL	LE to ON										
tPZH	Output Enable Time		1.5	9.5	1.5	6.5	1.5	5.5	1.5	4.8	ns
tPZL											
tPHZ	Output Disable Time		1.5	6.5	1.5	5.5	1.5	5.0	1.5	4.0	ns
tPLZ											
tSU	Set-up Time HIGH or LOW, DN to LE	2.0	—	2.0	—	2.0	—	1.5	—	ns	
tH	Hold Time HIGH or LOW, DN to LE	1.5	—	1.5	—	1.5	—	1.0	—	ns	
tW	LE Pulse Width HIGH	6.0	—	5.0	—	5.0	—	3.0	—	ns	

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.