National Semiconductor

PRELIMINARY

54ABT/74ABT377C
Octal D-Type Flip-Flop with Clock Enable

General Description

The 'ABT377C has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

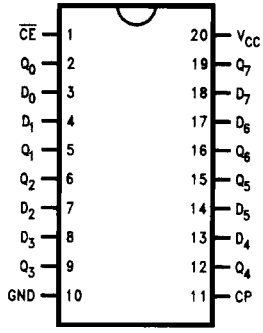
Features

- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- See 'ABT273C for master reset version
- See 'ABT373C for transparent latch version
- See 'ABT374C for TRI-STATE® version
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed 2000V minimum ESD protection
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention

Ordering Code: See Section 10

Connection Diagrams

Pin Assignment for DIP, SOIC SSOP and Flatpak



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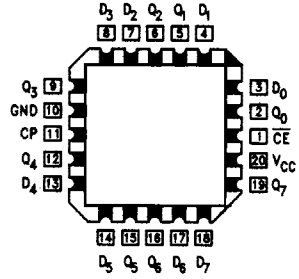
Pin Assignment for LCC



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Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

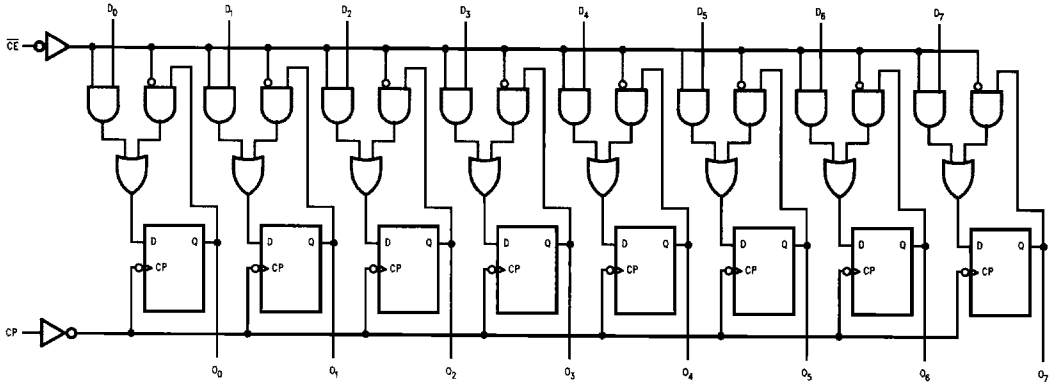
Truth Table

Mode Select-Function Table

Operating Mode	Inputs			Output
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	⌐‾	l	h	H
Load "0"	⌐‾	l	l	L
Hold	⌐‾	h	X	No Change
(Do Nothing)	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
⌐‾ = LOW-to-HIGH Clock Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-Off State	−0.5V to +4.75V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	2000V
DC Latchup Source Current	−500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT377C Min	ABT377C Typ	ABT377C Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0					I_{OH} = −24 mA
		74ABT	2.0					I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (Note 2)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (Note 2)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCT}	Maximum I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}	No Load			0.1	mA/MHz	Max	Outputs Open (Note 1) One bit Toggling, 50% Duty Cycle

Note 1: For 8 bits toggling, I_{CCD} < 0.5 mA/MHz.

Note 2: Guaranteed but not tested.

AC Electrical Characteristics: See Section 2 (SOIC package, contact factory for DIP or SSOP)

Symbol	Parameter	74ABTC $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54ABTC $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency								MHz	
t_{PLH}	Propagation Delay CP to O_n	2.2		6.5			2.2	6.5	ns	2–3, 5
t_{PHL}		3.1		7.3			3.1	7.3		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABTC $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		54ABTC $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		74ABTC $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH	2.0				2.0		ns	2–6
$t_s(L)$	or LOW D_n to CP	2.0				2.0			
$t_h(H)$	Hold Time, HIGH	1.8				1.8		ns	2–6
$t_h(L)$	or LOW D_n to CP	1.8				1.8			
$t_s(H)$	Setup Time, HIGH	3.0				3.0		ns	2–6
$t_s(L)$	or LOW $\overline{CE}$ to CP	3.0				3.0			
$t_h(H)$	Hold Time, HIGH	1.8				1.8		ns	2–6
$t_h(L)$	or LOW $\overline{CE}$ to CP	1.8				1.8			
$t_w(H)$	Pulse Width, CP,	3.3				3.3		ns	2–3
$t_w(L)$	HIGH or LOW	3.3				3.3			

Capacitance (SOIC package, contact factory for DIP or SSOP) (Note 3)

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$, $T_A = 25°C$
C_{OUT} (Note 1)	Output Capacitance	9	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.