



# HIGH-SPEED CMOS QUAD 2-INPUT MULTIPLEXER

**IDT74FCT158T**

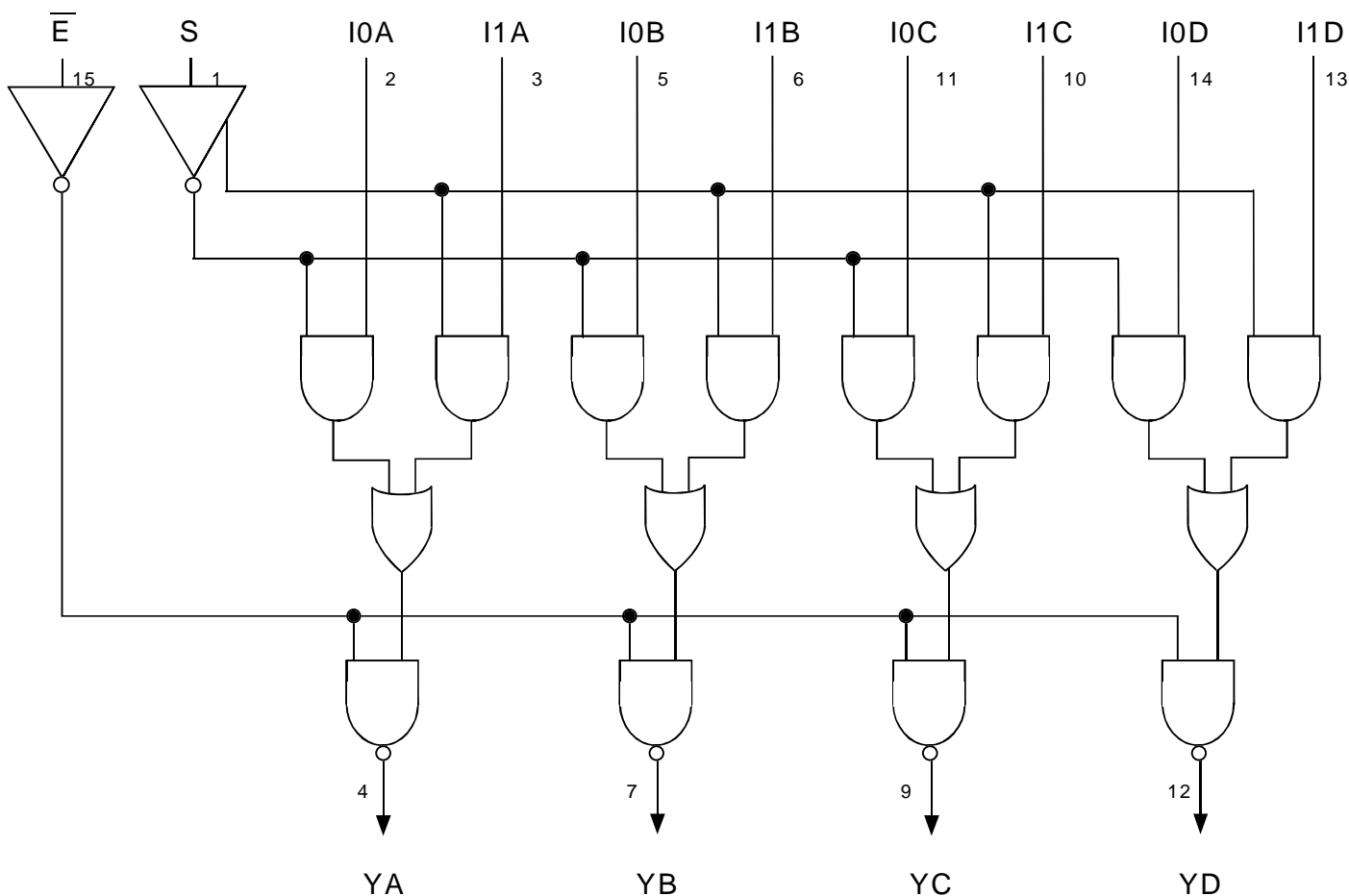
## FEATURES:

- Pin and function compatible to the Quality QS74FCT Family
- Extended commercial range of -40°C to +85°C
- CMOS power levels: <7.5mW static
- Available in SOIC and QSOP packages
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- JEDEC-FCT spec compatible
- A and C speed grades with 4.3ns for C
- I<sub>OL</sub> = 48mA

## DESCRIPTION:

The IDT74FCT158T is an inverting, high-speed CMOS TTL-compatible, quad, 2-input multiplexer with TTL outputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when V<sub>CC</sub> is removed from the device.

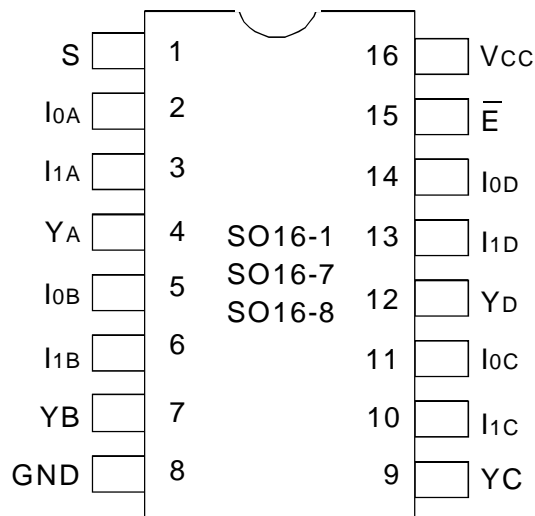
## Functional Block Diagram



**EXTENDED COMMERCIAL TEMPERATURE RANGE**

**JULY 1999**

## PIN CONFIGURATION



150mil SOIC/ 300mil SOIC/ QSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Symbol	Description	Max.	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	- 0.5 to +7.0	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	- 0.5 to +7.0	V
TSTG	Storage Temperature	- 65 to +150	°C
I <sub>OUT</sub>	DC Output Current	120	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	- 20	mA
I <sub>OK</sub>		- 50	mA

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

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### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	I/O	Description
I <sub>xx</sub>	I	Data Inputs
S	I	Select Inputs
E-bar	I	Enable Input (Active LOW)
Y <sub>x</sub>	O	Data Outputs

## FUNCTION TABLE

E-bar	S	YA	YB	YC	YD	Function
H	X	H	H	H	H	Disable
L	L	I0A-bar	I0B-bar	I0C-bar	I0D-bar	Select 0
L	H	I1A-bar	I1B-bar	I1C-bar	I1D-bar	Select 1

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for all inputs		—	0.2	—	V
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$I_{IL}$	Input LOW Current						
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$		-60	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^\circ\text{C}^{(3)}$		—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -15\text{mA}$	2.4	—	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 48\text{mA}$	—	—	0.5	V

### NOTES:

1. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
3. This parameter is guaranteed but not tested.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(2)}$ freq = 0 <sup>(2)</sup>	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/MHz

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### NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} \text{DH} + I_{CCD} (\text{fCP}/2 + \text{fiNi})$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4\text{V})$   
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$   
 $\text{NT} = \text{Number of TTL Inputs at DH}$   
 $I_{CCD} = \text{Dynamic Current Caused by an Output Transition Pair (HLH or LHL)}$   
 $\text{fCP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $\text{fi} = \text{Input Frequency}$   
 $\text{Ni} = \text{Number of Inputs at fi}$   
 All currents are in milliamps and all frequencies are in megahertz.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE(1)**

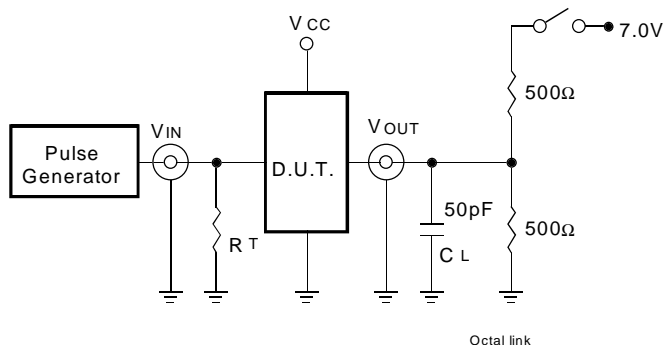
Symbol	Parameter <sup>(2)</sup>	74FCT158AT		74FCT158CT		Unit
		Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay I <sub>xx</sub> to Y <sub>x</sub>	1.5	5	1.5	4.3	ns
tPLH tPHL	Propagation Delay S to Y <sub>x</sub>	1.5	7	1.5	5.2	ns
tPLH tPHL	Propagation Delay $\bar{E}$ to Y <sub>x</sub>	1.5	6	1.5	4.8	ns

**NOTES:**

1. C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.
2. Minimums guaranteed but not tested.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

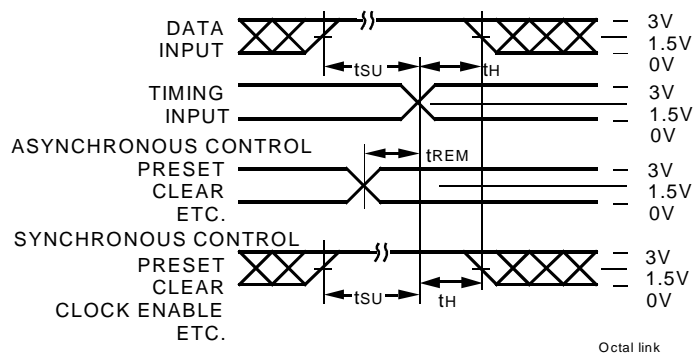
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

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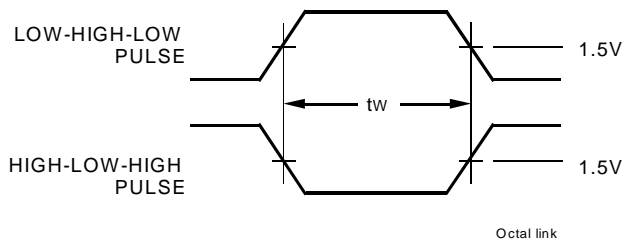
#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

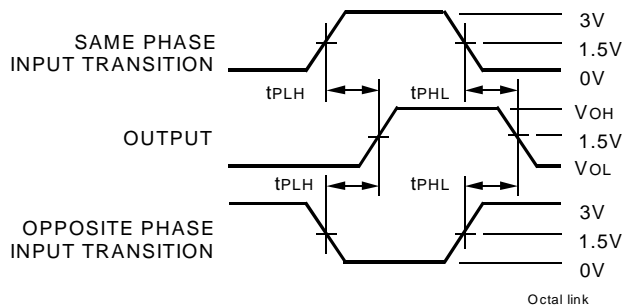
### SET-UP, HOLD, AND RELEASE TIMES



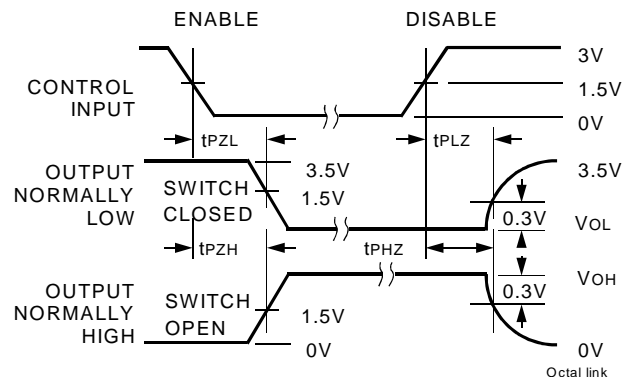
### PULSE WIDTH



### PROPAGATION DELAY



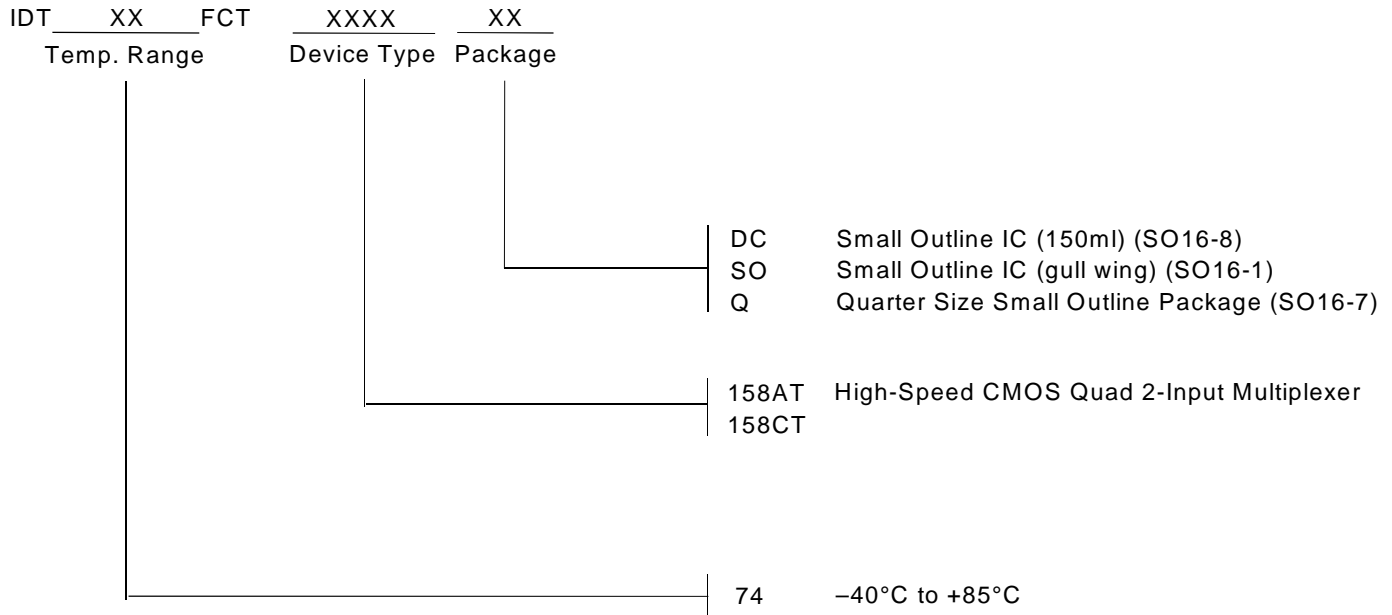
### ENABLE AND DISABLE TIMES



#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>f</sub> ≤ 2.5ns

**ORDERING INFORMATION**



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