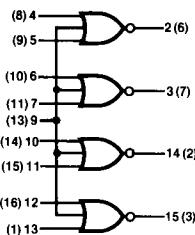


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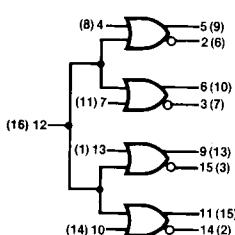
LOGIC DIAGRAMS

V_{CC1} = Pin 1(5), V_{CC2} = Pin 16(4), V_{EE} = Pin 8(12), () = Flatpak

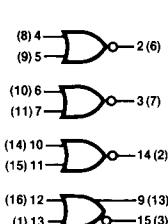
F10100/F10500



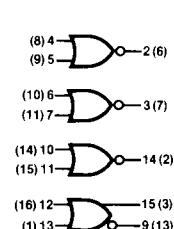
F10101/10501



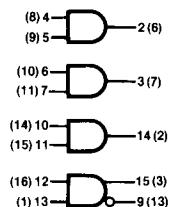
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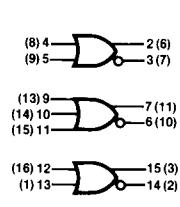
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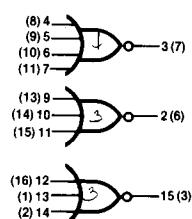
F10104/10504



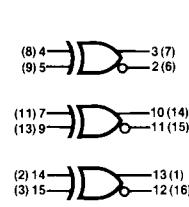
F10105/10505



F10106/10506

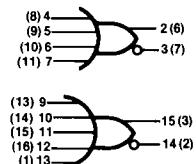


F10107/10507

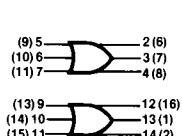


V_{CC1} = Pin 1 (5)
 V_{CC2} = Pin 16 (4)
 V_{EE} = 8 (12)

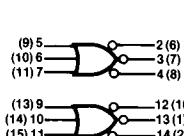
F10109/10509



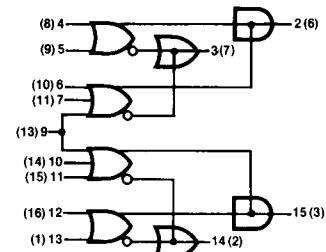
F10110/10510



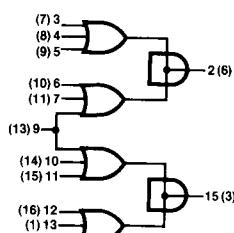
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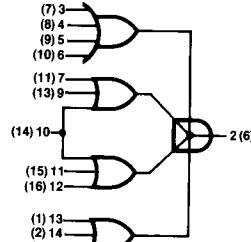
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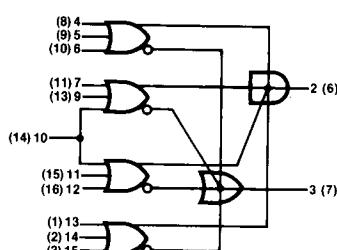
F10118/10518



F10119/10519



F10121/10521



F10K SERIES
GATE FAMILY SPECIFICATIONS

DC CHARACTERISTICS: $V_{EE} = -5.2\text{ V}$, $V_{CC} = \text{GND}$

F10100	•	F10500	•	F10101	•	F10501	•	F10102	•	F10502
F10103	•	F10503	•	F10104	•	F10504	•	F10105	•	F10505
F10106	•	F10506	•	F10107	•	F10507	•	F10109	•	F10509
F10110	•	F10510	•	F10111	•	F10511	•	F10118	•	F10518
F10119	•	F10519	•	F10121	•	F10521				

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	TA	CONDITIONS
		B	TYP	A			
I_{IH}	All Input Current HIGH's are 265, unless otherwise noted				μA	25°C	$V_{IN} = V_{IHA}$
	F10100 Pin 9			550			
	F10101 Pin 12			550			
	F10103 All Inputs			245			
	F10104 Pins 4, 6, 10, 12			220			
	F10107 Pins 5, 7, 15			220			
	F10110 All Inputs			425			
	F10111 All Inputs			425			
	F10118 Pin 9			370			
	F10119 Pin 10			370			
	F10121 Pin 10			370			
I_{EE}	Power Supply Current				mA	25°C	Inputs and Outputs Open
	F10100	-26	-21				
	F10101	-26	-20				
	F10102	-26	-20				
	F10103	-26	-20				
	F10104	-35	-28				
	F10105	-21	-15				
	F10106	-21	-15				
	F10107	-28	-22				
	F10109	-14	-10				
	F10110	-38	-28				
	F10111	-38	-28				
	F10118	-26	-20				
	F10119	-26	-20				
	F10121	-26	-20				

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2\text{ V}$, $T_A = 25^\circ\text{C}$

F10100	•	F10101	•	F10102	•	F10103	•	F10105	•	F10106	•	F10109
F10500	•	F10501	•	F10502	•	F10503	•	F10505	•	F10506	•	F10509

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH} t_{PHL}	Propagation Delay	1.0	2.0	2.9	ns	See Figure 1
t_{TLH} t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.2	3.3	ns	See Figure 1

FAIRCHILD ECL • F10K SERIES

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25^\circ\text{C}$

F10104 • F10504

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay Inputs 5, 6, 11, 12	1.4	2.2	3.4	ns	
t_{PHL}, t_{PLH}	Propagation Delay, Inputs 4, 7, 10, 13	1.4	2.9	3.7	ns	
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.2	3.5	ns	

See Figure 1

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25^\circ\text{C}$

F10107 • F10507

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay	1.1	2.4	3.7	ns	
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.5	3.5	ns	

See Figure 1

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SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25^\circ\text{C}$

F10110 • F10510 • F10111 • F10511

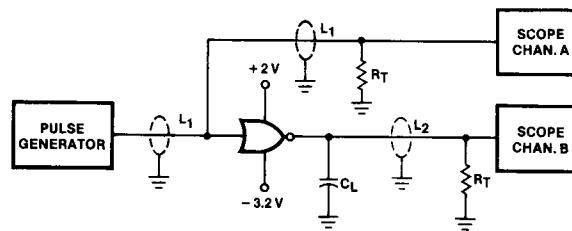
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay	1.4	2.4	3.5	ns	
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.2	3.5	ns	

See Figure 1

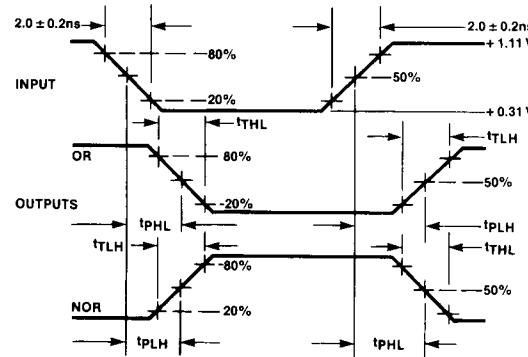
SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25^\circ\text{C}$ F10118 • F10518 • F10119 • F10519 • F10121 • F10521

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	Typ	A		
t_{PLH} , t_{PHL}	Propagation Delay	1.4	2.3	3.4	ns	See Figure 1
t_{TLH} t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.2	4.0	ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
 R_T = 50 Ω termination of scope
 C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}



Jig set-up with no circuit under test
 $V_{CC1} = V_{CC2} = 2.0$ V
 $V_{EE} = -3.2$ V

Fig. 1