

# HD74LV245

## Octal Bidirectional Transceivers with 3-state Outputs

### Description

The HD74LV245 has eight buffers with three state outputs in a 20 pin package. When (DiR) is high, data flows from the A inputs to the B outputs, and when (DiR) is low, data flows from the B inputs to the A outputs. A and B bus are separated by making enable input ( $\overline{OE}$ ) high level. Low voltage operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

### Features

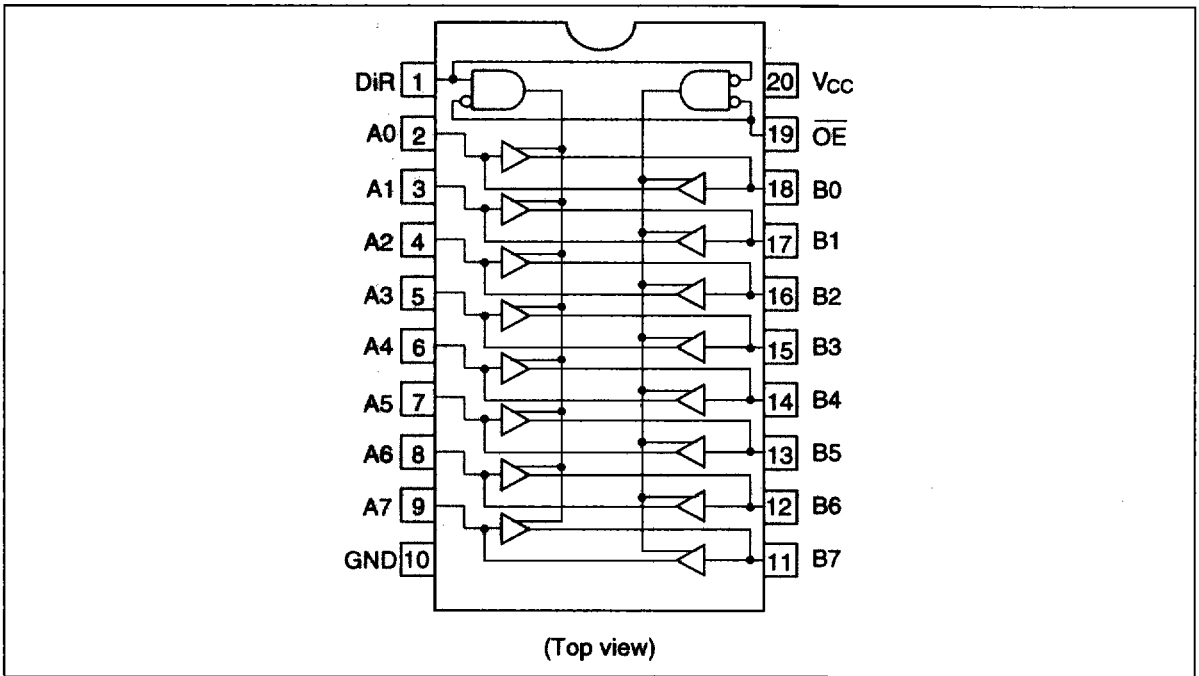
- $V_{CC} = 2.0\text{ V to }5.5\text{ V}$
- All inputs  $V_{IH}(\text{Max.}) = 5.5\text{ V} (@V_{CC} = 0\text{ V to }5.5\text{ V})$
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V} (@V_{CC} = 3.3\text{ V}, T_a = 25^\circ\text{C})$
- Typical  $V_{OH}$  undershoot  $> 2.0\text{ V} (@V_{CC} = 3.3\text{ V}, T_a = 25^\circ\text{C})$
- Output current  $\pm 8\text{ mA} (@V_{CC} = 3.0\text{ V to }3.6\text{ V})$   
 $\pm 16\text{ mA} (@V_{CC} = 4.5\text{ V to }5.5\text{ V})$

### Function Table

$\overline{OE}$	Inputs		Operation
		DiR	
L		L	B data to A bus
L		H	A data to B bus
H		X	Z

H: High level  
L: Low level  
Z: High impedance  
X: Immaterial

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 7.0	V	
Input diode current	$I_{IK}$	-20	mA	$V_i = -0.5$ V
Input voltage	$V_i$	-0.5 to 7.0	V	DiR, $\overline{OE}$
		-0.5 to $V_{CC} + 0.5$	V	A0 to A7, B0 to B7
Output diode current	$I_{OK}$	-50	mA	$V_o = -0.5$ V
		50	mA	$V_o = V_{CC} + 0.5$ V
Output voltage	$V_o$	-0.5 to $V_{CC} + 0.5$	V	
Output current	$I_o$	$\pm 35$	mA	
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	70	mA	
Storage temperature	Tstg	-65 to +150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

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### Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	2.0 to 5.5	V	
Input / output voltage	$V_I$	0 to 5.5	V	DiR, $\overline{OE}$
	$V_{VO}$	0 to $V_{CC}$	V	A0 to A7, B0 to B7
Operating temperature	$T_a$	-40 to 85	°C	
Output current	$I_{OH}$	-8	mA	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$
		$-16^{*2}$	mA	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$
	$I_{OL}$	8	mA	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$
		$16^{*2}$	mA	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$
Input rise / fall time <sup>1)</sup>	$t_r, t_f$	50	ns/V	$V_{CC} = 5.5\text{ V}$
		100	ns/V	$V_{CC} = 3.6\text{ V}$

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform : Refer to test circuit of switching characteristics.

2. duty cycle  $\leq 50\%$

Electrical Characteristics

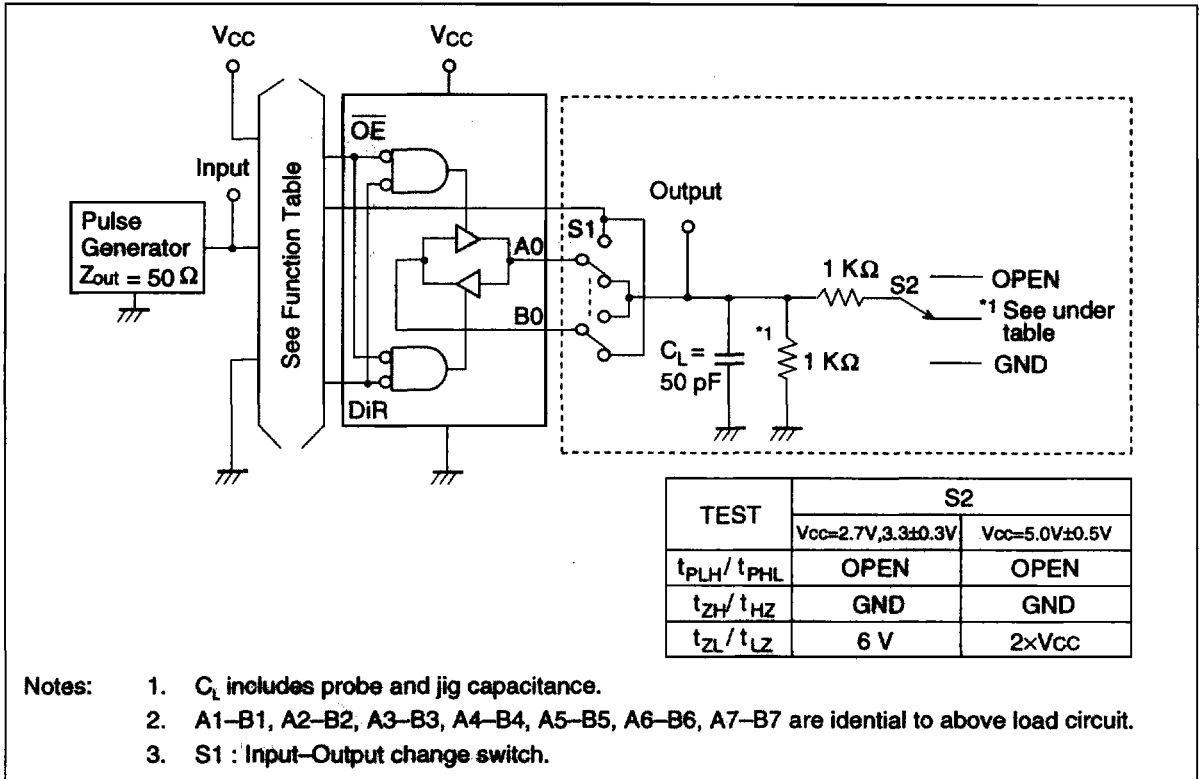
Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V <sub>IH</sub>	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	V <sub>CC</sub> ×0.7	—	V	
	V <sub>IL</sub>	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	V <sub>CC</sub> ×0.3	V	
Output voltage	V <sub>OH</sub>	2.7 to 5.5	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA
		3.0	2.4	—	V	I <sub>OH</sub> = -8 mA
		4.5	3.6	—	V	I <sub>OH</sub> = -16 mA
	V <sub>OL</sub>	2.7 to 5.5	—	0.2	V	I <sub>OL</sub> = 100 μA
		3.0	—	0.4	V	I <sub>OL</sub> = 8 mA
		4.5	—	0.5	V	I <sub>OL</sub> = 16 mA
Input current	I <sub>IN</sub>	0 to 5.5	—	±1.0	μA	V <sub>IN</sub> ( $\overline{OE}$ , DIR) = 5.5 V or GND V <sub>IN</sub> = V <sub>CC</sub> or GND (A0 to A7 or B0 to B7)
Off state output current	I <sub>OZ</sub>	5.5	—	±5.0	μA	V <sub>IN</sub> = V <sub>CC</sub> , GND V <sub>OUT</sub> = V <sub>CC</sub> or GND
Quiescent supply current	I <sub>CC</sub>	5.5	—	20	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	3.0 to 3.6	—	500	μA	V <sub>IN</sub> = one input at (V <sub>CC</sub> - 0.6) V, other inputs at V <sub>CC</sub> or GND

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## Switching Characteristics

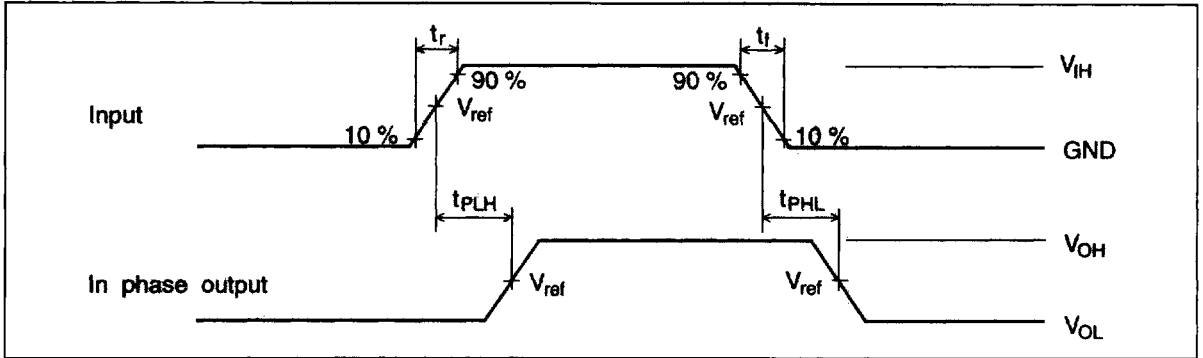
Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$			Unit	From (Input)	To (Output)
			Min	Typ	Max	Min	Typ	Max			
Propagation delay time	$t_{PLH}$	2.7	—	9.5	14.5	1.0	—	16.0	ns	A or B	B or A
	$t_{PHL}$	$3.3 \pm 0.3$	—	7.5	13.0	1.0	—	14.5	ns		
		$5.0 \pm 0.5$	—	5.5	9.5	1.0	—	10.5	ns		
Enable time	$t_{ZH}$	2.7	—	14.5	21.0	1.0	—	23.5	ns	$\overline{OE}$	A or B
	$t_{ZL}$	$3.3 \pm 0.3$	—	12.0	18.5	1.0	—	20.5	ns		
		$5.0 \pm 0.5$	—	8.0	14.0	1.0	—	15.5	ns		
Disable time	$t_{HZ}$	2.7	—	13.0	18.5	1.0	—	20.0	ns	$\overline{OE}$	A or B
	$t_{LZ}$	$3.3 \pm 0.3$	—	12.0	17.0	1.0	—	18.5	ns		
		$5.0 \pm 0.5$	—	8.0	13.5	1.0	—	14.5	ns		
Input capacitance	$C_{IN}$	$3.3 \pm 0.3$	—	—	—	—	2.5	—	pF	$\overline{OE}$ , DiR	
Input / Output capacitance	$C_{IO}$	$3.3 \pm 0.3$	—	—	—	—	7.0	—	pF	A, B	

Test Circuit

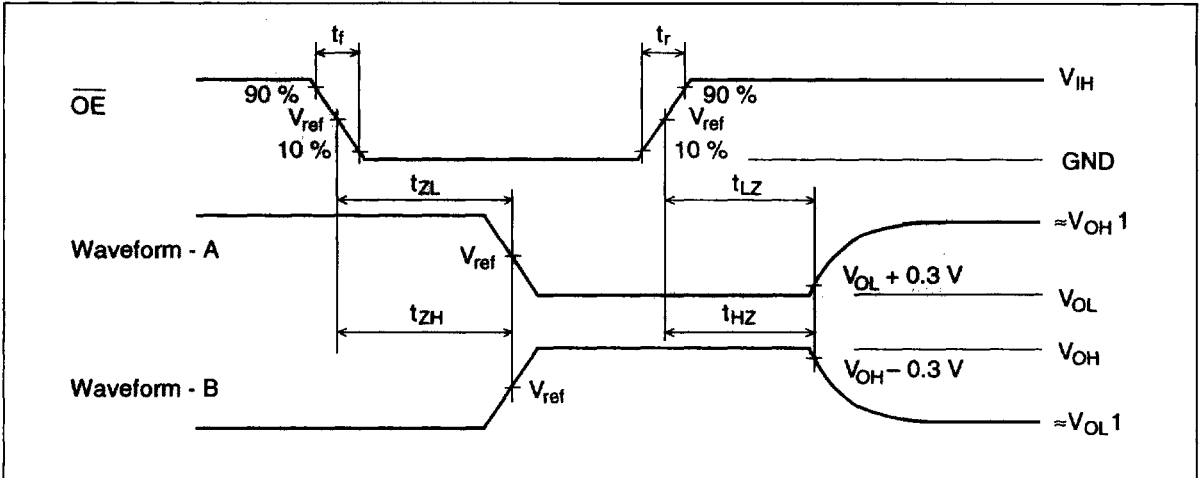


# HD74LV245

## Waveforms-1



## Waveforms-2



Symbol	$V_{CC}=2.7V, 3.3\pm 0.3V$	$V_{CC}=5.0V\pm 0.5V$
$V_{IH}$	2.7 V	$V_{CC}$
$V_{ref}$	1.5 V	$50\%V_{CC}$
$V_{OH1}$	3 V	$V_{CC}$
$V_{OL1}$	GND	GND

- Notes:
- $t_r = 2.5 \text{ ns}$ ,  $t_f = 2.5 \text{ ns}$
  - Input waveform : PRR = 10 MHz, duty cycle 50%
  - Waveform - A shows input conditions such that the output is "L" level when enable by the output control.
  - Waveform - B shows input conditions such that the output is "H" level when enable by the output control.