Low-Cost, Quad, SPST, CMOS Analog Switches

Features

- Low On-Resistance
- On-Resistance Matching Between Channels, 0.2Ω typ
- On-Resistance Flatness, <2Ω typ
- Low Off-Channel Leakage, <100pA @ +25°C
- TTL/CMOS Logic Compatible
- GND-to-V+ Analog Signal Dynamic Range
- Low Power Consumption (<12µW)
- Low Crosstalk: -86dB @ 1MHz
- Low Off-Isolation: -58dB @ 1 MHz
- Wide Bandwidth: > 100 MHz
- Small QSOP-16 Package Saves Board Area

Applications

- Instrumentation, ATE
- Sample-and-Holds
- Audio Switching and Routing
- Telecommunication Systems
- PBX, PABX
- Battery-Powered Systems

Description

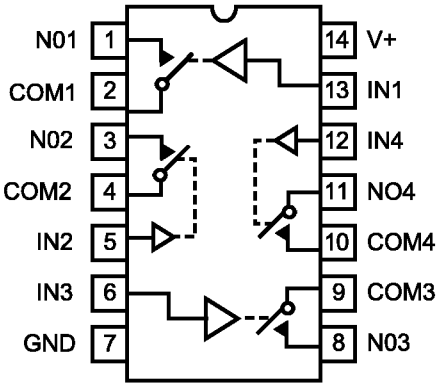
The PS4066/PS4066A are improved SPST CMOS analog switches ideal for low-distortion audio switching. These high precision, medium voltage switches were designed to operate with single-supplies from +3V to 16V. They are fully specified with +12V, +5V, and +3V supplies. The PS4066/PS4066A has four normally open (NO) switches. Each switch conducts current equally well in either direction when on. In the off state each switch blocks voltages up to the power-supply rails.

With +12V power supply, the PS4066/PS4066A guarantee <45Ω on-resistance. On-resistance matching between channels is within 2Ω (PS4066). On-resistance flatness is less than 4Ω (PS4066A) over the specified range. The PS4066A guarantees low leakage currents (<100pA @ 25°C, <6nA @ +85°C) and fast switching speeds (t_{ON} < 175ns). ESD sensitivity rating is >2,000V per MIL-STD 883, Method 3015.7

Both devices are available in PDIP-14, narrow-body SOIC-14, and QSOP-16 packages. Available temperature ranges are: commercial (0°C to 70°C), and industrial (-40°C to +85°C).

For operation below 5V, the PI5A101/PI5A391/PI5A392 are also recommended.

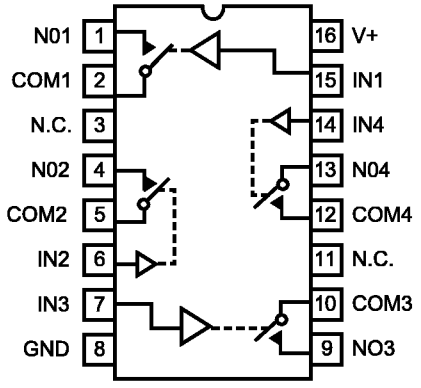
Functional Diagrams, Pin Configurations, and Truth Table



Top View
PDIP/SO

Logic	Switch
0	OFF
1	ON

N.C. = No Internal Connection
Switches shown for logic "0" input



Top View
QSOP

Absolute Maximum Ratings

Voltages Referenced to GND
V+ ..... -0.3V to +17V
V_{IN}, V_{COM}, V_{NC}, V_{NO} (Note 1) ..... -2V to (V+) +2V
or 30mA, whichever occurs first
Current (any terminal) 30mA
Peak Current, COM, NO, NC
(pulsed at 1ms, 10% duty cycle) 100mA
ESD per Method 3015.7 ..... >2000V

Thermal Information

Continuous Power Dissipation (T_A= +70°C)
Plastic DIP (derate 10.5mW/°C above +70°C) 800mW
SO and QSOP (derate 8.7mW/°C above +70°C) 650mW
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note
Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Single +12V Supply

(V+ = 12V ±10%, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions		Temp. (°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch								
Analog Signal Range(3)	V_{ANALOG}			Full	0		V+	V
On Resistance	R_{ON}	V+ = 12V, I_{COM} = 2mA, V_{NO} = 10V		25		12	45	Ω
				Full			55	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ = 12V, I_{COM} = 2mA V_{NO} = 10V	PS4066 PS4066A	25		0.5 0.5	4 2	
				Full			6	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V+ = 12V, I_{COM} = 2mA, V_{NO} = 10V, 5V, 1V		25		2	4	
				Full			6	
NO or NC Off Leakage Current(6)	$I_{NO(OFF)}$ OR $I_{NC(OFF)}$	V+ = 12V, V_{COM} = 0V, V_{NO} = 10V	PS4066 PS4066A	25	-1 -0.1		1 0.1	nA
				Full	-6		6	
COM Off Leakage Current(6)	$I_{COM(OFF)}$	V+ = 12V, V_{COM} = 0V, V_{NO} = 10V	PS4066 PS4066A	25	-1 -0.1		1 0.1	
				Full	-6		6	
COM On Leakage Current(6)	$I_{COM(ON)}$	V+ = 12V, V_{COM} = 10V, V_{NO} = 10V	PS4066 PS4066A	25	-2 -0.2		2 0.2	
				Full	-12		12	

Electrical Specifications - Single +12V Supply (continued)

(V+ = 12V ±10%, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Logic Input							
Input Current with Input Voltage High	I_{INH}	IN =5V, all others = 0.8V	Full	-0.5	0.005	0.5	µA
Input Current with Input Voltage Low	I_{INL}	IN = 0.8V, all others =5V	Full	-0.5	0.005	0.5	µA
Dynamic							
Turn-On Time	t_{ON}	V_{COM} = 10V, Figure 2	25		45	100	ns
			Full			150	ns
Turn-Off Time	t_{OFF}		25		17	75	ns
			Full			100	ns
On-Channel Bandwidth	BW	Signal = 0dbm Figure 4, 50Ω in and out	25		100		MHz
Charge Injection(3)	Q	C_L=1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 3	25		2	10	pC
Off Isolation	OIRR	R_L = 50Ω, C_L= 5pF, f = 1 MHz, Figure 4	25		-58		dB
Crosstalk(8)	X_{TALK}	R_L = 50Ω, C_L= 5pF, f = 1 MHz, Figure 5	25		-86		dB
NO Capacitance	$C_{(OFF)}$	f =1 MHz, Figure 6	25		9		pF
COM Off Capacitance		f =1 MHz, Figure 6	25		9		pF
COM On Capacitance	$C_{COM(ON)}$	f =1MHz, Figure 7	25		22		pF
Supply							
Positive Supply Current	I+	V_{IN} = 0V or V+, all channels on or off	Full	-1	0.001	1	µA
Total Harmonic Distortion	THD		Full		0.03		%

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = \Delta R_{ON}$ max - ΔR_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NO})], V_{COM} = 0utput, V_{NC} /V_{NO} = input to off switch
8. Between any two switches.

Electrical Specifications - Single +5V Supply

(V+ = +5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions		Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch								
Analog Signal Range(3)	V_{ANALOG}			Full	0		V+	V
On-Resistance	R_{ON}	V+ = 4.5V, I_{COM} = -1mA, V_{NO} = 3.5V		25		22	75	Ω
				Full			100	
On-Resistance MatchBetween Channels(4)	ΔR_{ON}	V+ =5V, I_{COM} = -1mA, V_{NO} = 3V		25		0.3	4	
				Full			12	
On-Resistance Flatness(3,5)	$R_{FLAT(ON)}$	V+ = 5V, I_{COM} = -1mA, V_{NO} = 1V, 3V		25		4	6	
				Full			8	
NO Off Leakage Current(9)	$I_{NO(OFF)}$	V+ = 5.5V, V_{COM} = 0V, V_{NO} = 4.5V	PS4066 PS4066A	25	-1 -0.1		1 0.1	nA
				Full	-6		6	
COM Off Leakage Curren(9)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 0V, V_{NO} = 4.5V	PS4066 PS4066A	25	-1 -0.1		1 0.1	
				Full	-6		6	
COM On Leakage Current(6)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 5V, V_{NO} = 4.5V	PS4066 PS4066A	25	-2 -0.2		2 0.2	
				Full	-12		12	
Dynamic								
Turn-On Time	t_{ON}	V_{NO}= 3V		25		65	125	ns
				Full			175	
Turn-Off Time	t_{OFF}			25		30	75	
				Full			125	
On-Channel Bandwidth	BW	Signal = 0dBm, 50Ω in and out Figure 4		25		100		MHz
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 3		25		1	10	pC
Supply								
Positive Supply Current	I+	V+ = 5.5V, V_{IN} = 0V or V+, all channels on or off		Full	-1		1	µA

Electrical Specifications - Single +3V Supply

(V+ = +2.7V to 3.3V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

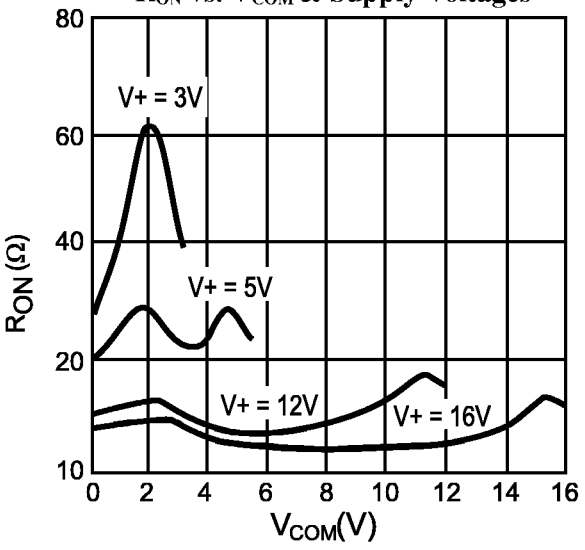
Parameter	Symbol	Conditions	Temp°C	Min.(1)	Typ(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
Channel On-Resistance	R_{ON}	V+ = 3V, I_{COM} = -1mA, V_{NO} = 1.5V	25			170	Ω
			Full			225	
Dynamic							
Turn-On-Time(3)	t_{ON}	V+ =3V, V_{NO} = 1.5V	25		80	185	ns
			Full			230	
Turn-Off-Time(3)	$t_{(OFF)}$	V+ =3V, V_{NO} = 1.5V	25		40	150	
			Full			200	
Charge Injection(3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0V	25		2	10	pC
Supply							
Positive Supply Current	I+	V+ = 3.3V, V_{IN} = 0V or V+, all channels on or off	Full	-1	0.001	1	µA

Notes:

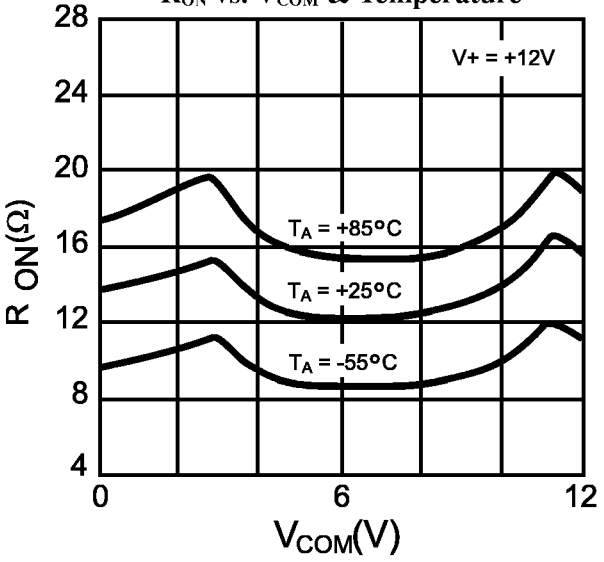
1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = \Delta R_{ON}$ max - ΔR_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NO})], V_{COM} = 0utput, V_{NC} /V_{NO} = input to off switch
8. Between any two switches.

Typical Operating Characteristics (TA = +25°C, unless otherwise noted)

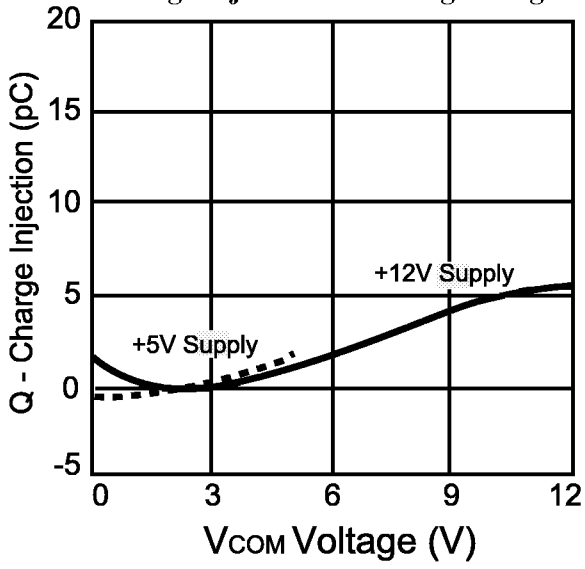
R_{ON} vs. V_{COM} & Supply Voltages



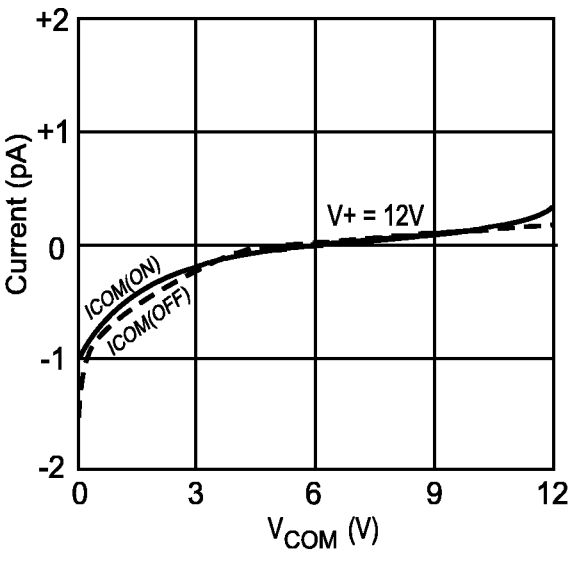
R_{ON} vs. V_{COM} & Temperature



Charge Injection vs. Analog Voltage

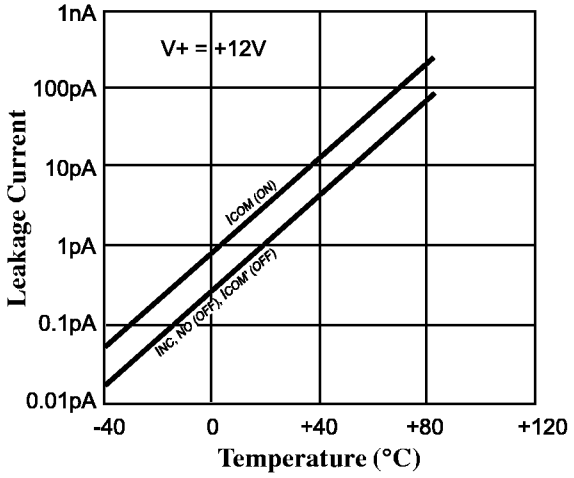


Leakage Currents vs. V_{COM}

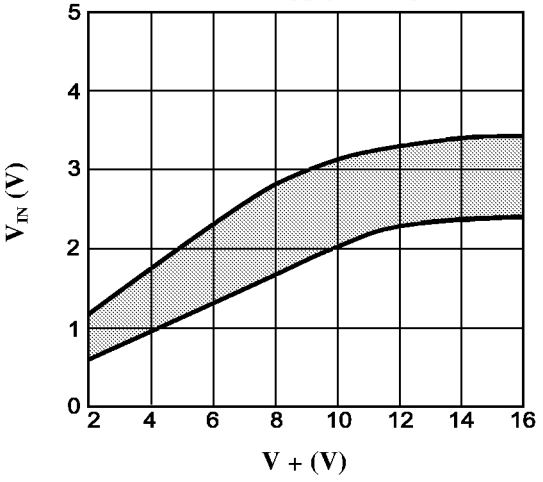


Typical Operating Characteristics (TA = +25°C, unless otherwise noted)

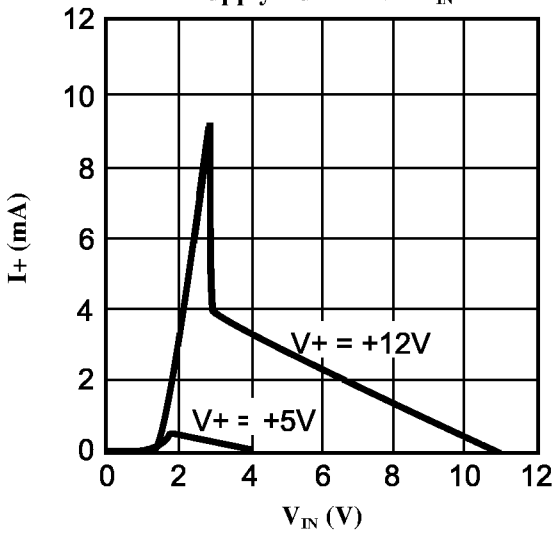
Leakage Current vs. Temperature



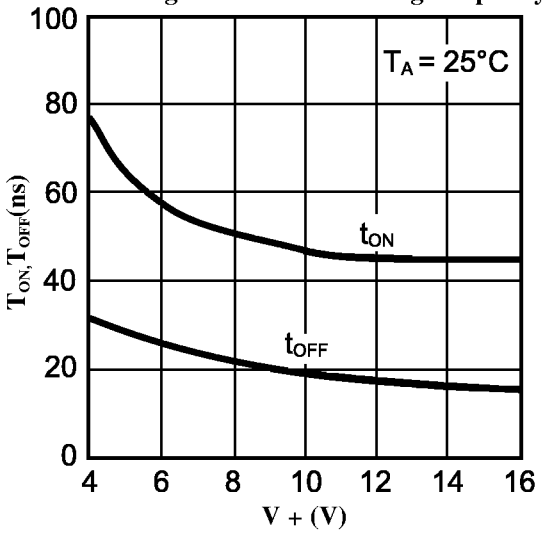
Input Switching Threshold vs. Supply Voltage



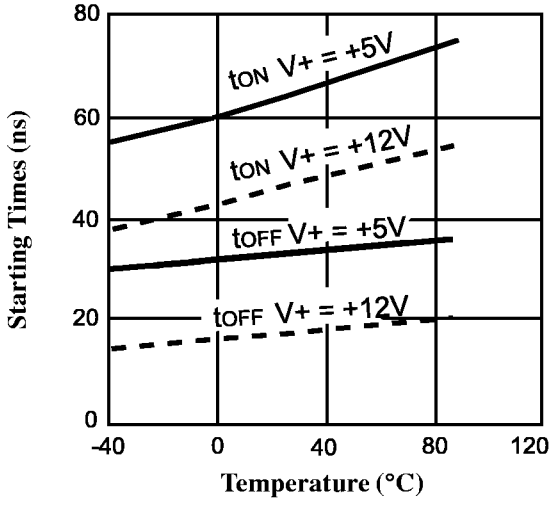
Supply Current vs. V_{IN}



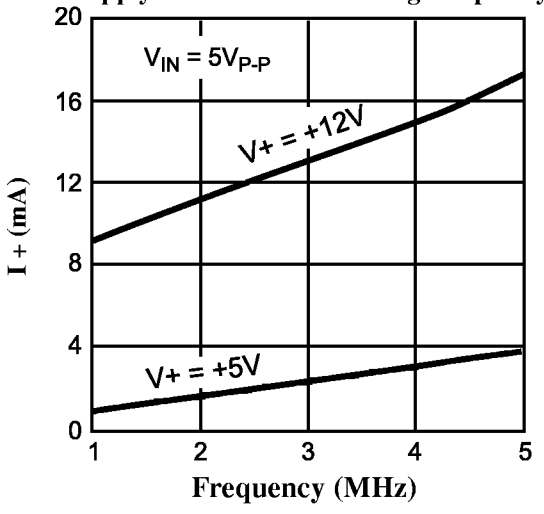
Switching Current vs. Switching Frequency



Switching Times vs. Temperature



Supply Currents vs. Switching Frequency



Pin Description

Applications Information

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, and then the logic inputs. If power-supply sequencing is not possible, add a small signal diode or current limiting resistor in series with the supply pin for overvoltage protection (Figure 1). Adding a diode reduces the analog signal range, but low switch resistance and low leakage characteristics are unaffected.

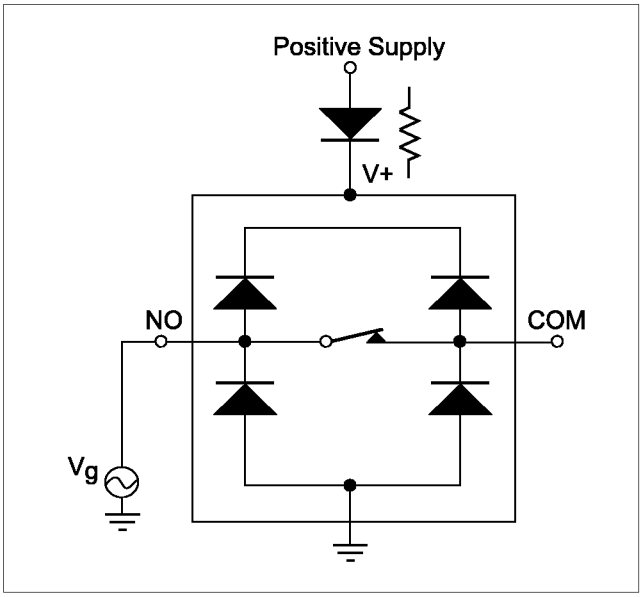


Figure 1. Overvoltage protection is accomplished using an external blocking diode or a current limiting resistor .

Test Circuits/Timing Diagrams

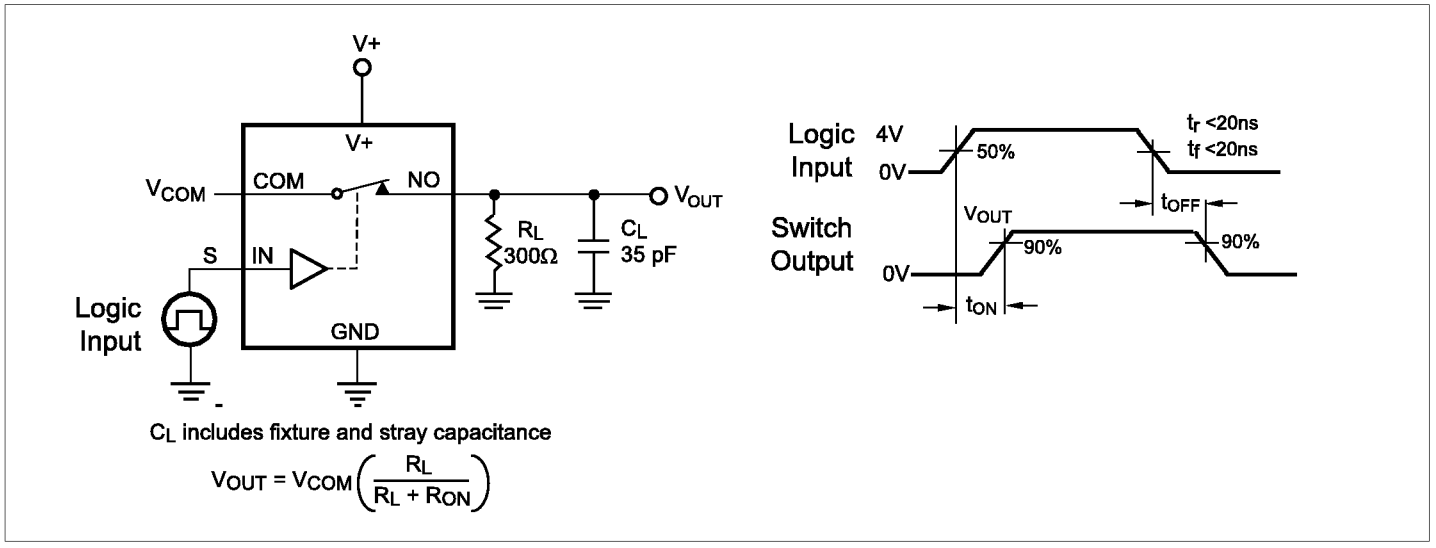


Figure 2. Switching Times

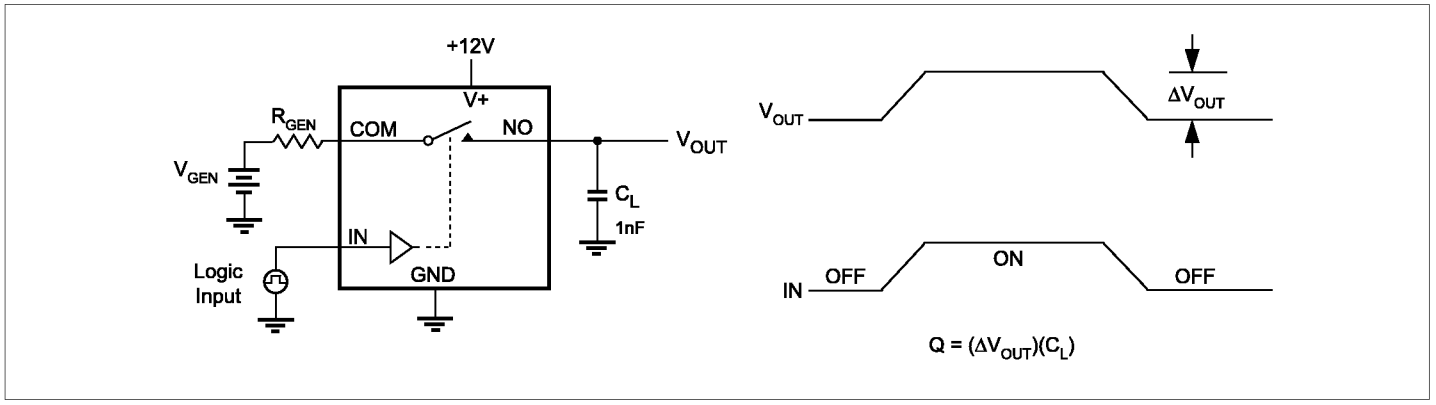


Figure 3. Charge Injection

Test Circuits/Timing Diagrams (continued)

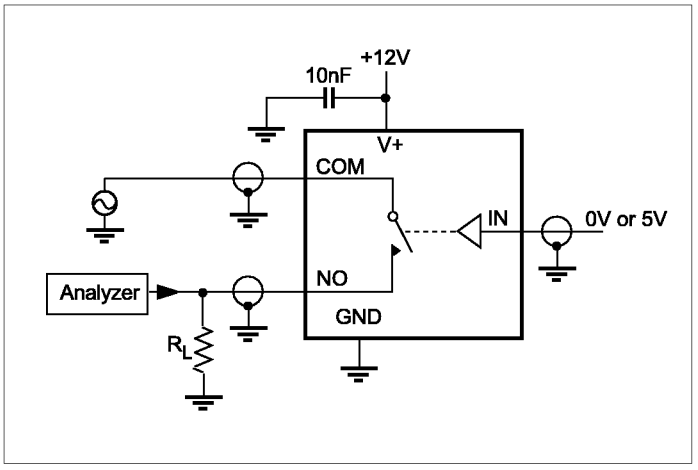


Figure 4. Off Isolation, BW

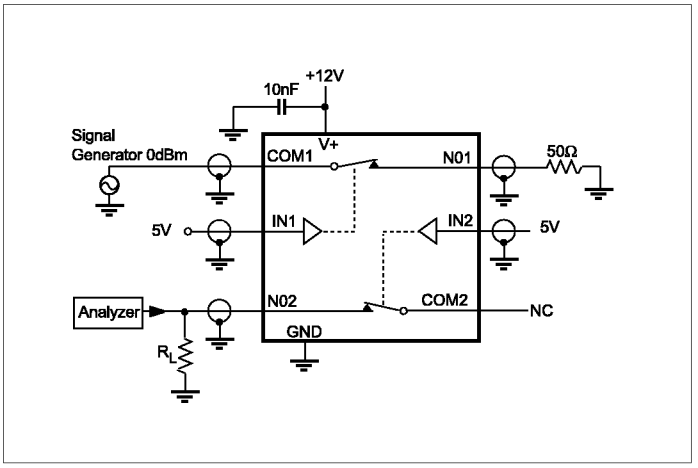


Figure 5. Crosstalk

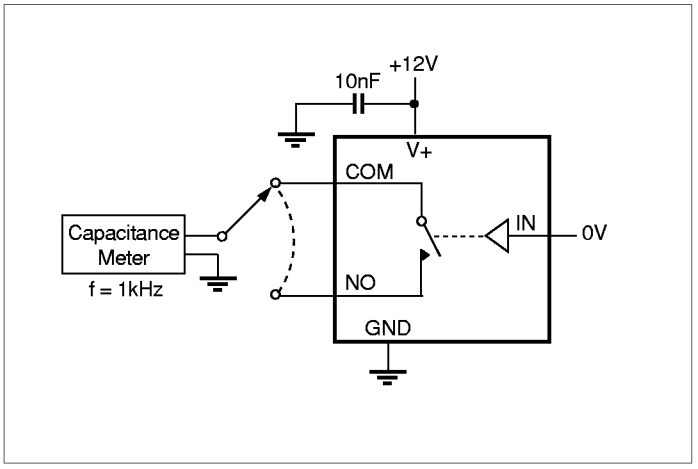


Figure 6. Channel-Off Capacitance

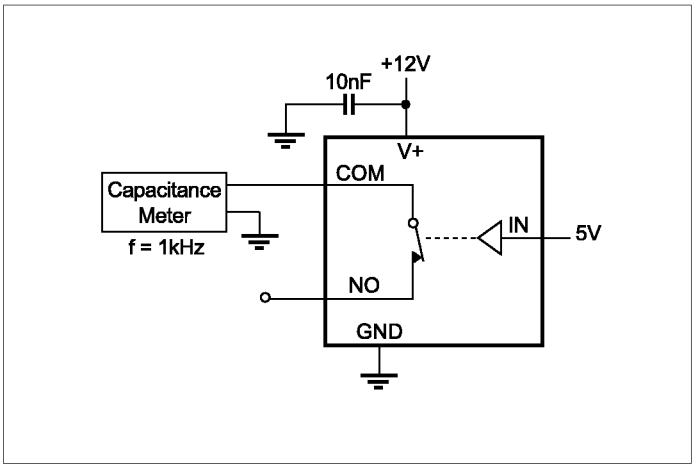


Figure 7. Channel-On Capacitance

Ordering Information

Part Number	Temperature - Range	Package
PS4066CPD	0ºC to + 70ºC	14 Plastic DIP
PS4066CSD	0ºC to + 70ºC	14 Narrow SO
PS4066CEE	0ºC to + 70ºC	16 QSOP
PS4066EPD	-40ºC to + 85ºC	14 Plastic DIP
PS4066ESD	-40ºC to + 85ºC	14 Narrow SO
PS4066ACPD	0ºC to + 70ºC	14 Plastic DIP
PS4066ACSD	0ºC to + 70ºC	14 Narrow SO
PS4066ACEE	0ºC to + 70ºC	16 QSOP
PS4066AEPD	-40ºC to + 85ºC	14 Plastic DIP
PS4066AESD	-40ºC to + 85ºC	14 Narrow SO
PS4066AEEE	-40ºC to + 85ºC	16 QSOP