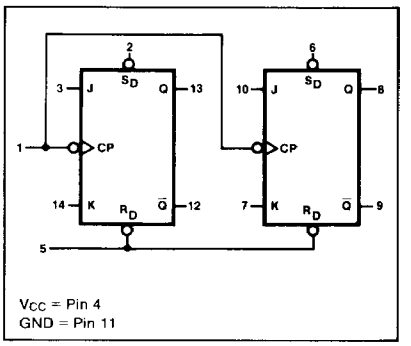
54LS/74LS78

DESCRIPTION

The "78" is a Dual JK Negative Edge-Triggered Flip-Flop featuring individual J, K, Set, common Clock and common Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when LOW, set or reset the outputs as shown in the Truth Table regardless of the levels at the other inputs. A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

LOGIC SYMBOL



V_{CC} = Pin 4
GND = Pin 11

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = -55°C to +125°C
Plastic DIP	Fig A	N74LS78N	
Ceramic DIP	Fig A	N74LS78F	S54LS78F
Flatpak	Fig A		S54LS78W

PIN CONFIGURATION

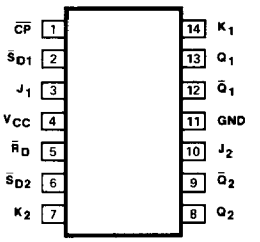


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS			54/74	54H/74H	54S/74S	54LS/74LS
$\overline{CP}$	Common Clock input	I_{IH} (μA) I_{IL} (mA)				160 -1.6
$\overline{R}_D$	Common Reset input	I_{IH} (μA) I_{IL} (mA)				120 -1.6
$\overline{S}_D$	Set input	I_{IH} (μA) I_{IL} (mA)				60 -0.8
JK	Data inputs	I_{IH} (μA) I_{IL} (mA)				20 -0.4
Q & $\overline{Q}$ Outputs		I_{OH} (μA) I_{OL} (mA)				-400 4/8 (a)

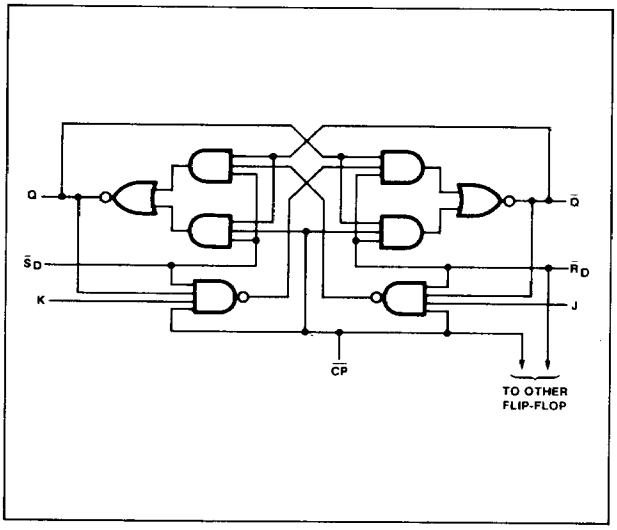
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current	V_{CC} = Max, V_{CP} = 0V								8.0	mA

NOTES

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\bar{S}_D$	$\bar{R}_D$	$\overline{CP}$	J	K	Q	$\bar{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\bar{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\bar{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH to LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH to LOW Clock transition.
q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition.
X = Don't care.

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS C_L = 15pF R_L = 2kΩ		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 4							30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 4								20 30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\bar{S}_D$ or $\bar{R}_D$ to output	Waveform 5								20 30	ns ns

AC SET-UP REQUIREMENTS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{W(H)}$	Clock pulse width (HIGH)	Waveform 4							20		ns
$t_{W(L)}$	Clock pulse width (LOW)	Waveform 4							13		ns
$t_{W(L)}$	Set or Reset pulse width (LOW)	Waveform 5							25		ns
t_s	Setup time J or K to Clock	Waveform 4							20		ns
t_h	Hold time J or K to Clock	Waveform 4							0		ns

NOTE

c. Both outputs will be HIGH while both $\bar{S}_D$ and $\bar{R}_D$ are LOW, but the output states are unpredictable if $\bar{S}_D$ and $\bar{R}_D$ go HIGH simultaneously.