54F/74F379

Quad Parallel Register With Enable

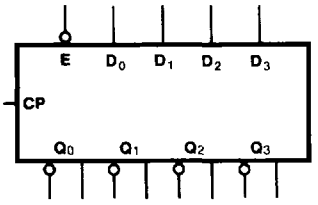
Description

The 'F379 is a 4-bit register with buffered common Enable. This device is similar to the 'F175 but features the common Enable rather than common Master Reset.

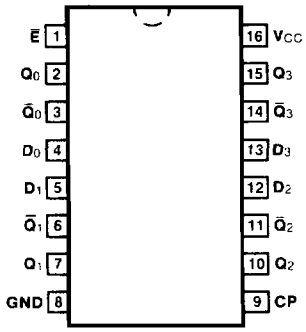
- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **Buffered Common Enable Input**
- **True and Complement Outputs**

Ordering Code: See Section 5

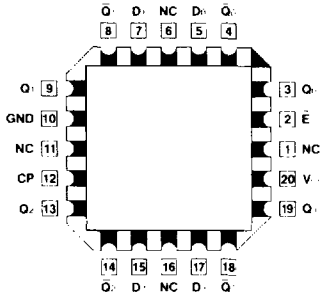
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
D_0-D_3	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
Q_0-Q_3	Flip-Flop Outputs	25/12.5
$\overline{Q}_0$-$\overline{Q}_3$	Complement Outputs	25/12.5

Functional Description

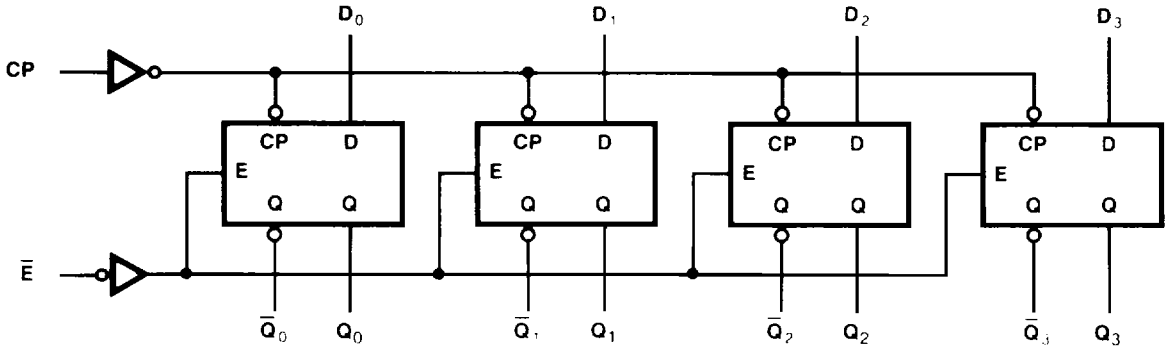
The 'F379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input. The D_n and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

Truth Table

Inputs			Outputs	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	↑	X	NC	NC
L	↑	H	H	L
L	↑	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		28	40	mA	V_{CC} = Max; D, $\overline{E}$ = Gnd, CP = ⌐

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140				100		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	4.0 5.0	5.0 6.5	6.5 8.5			4.0 5.0	7.5 9.5	ns	3-1 3-7

4

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	3.0 3.0					3.0 3.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	1.0 1.0					1.0 1.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{E}$ to CP	6.0 6.0					6.0 6.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{E}$ to CP	0 0					0 0			
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 5.0					4.0 5.0		ns	3-7