



# 3.3V CMOS 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS AND 5 VOLT TOLERANT I/O

**IDT74LVCR16952A**

## FEATURES:

- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- CMOS power levels ( $0.4\mu W$  typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP, TSSOP, and TVSOP packages

## DRIVE FEATURES:

- Balanced Output Drivers:  $\pm 12mA$
- Low switching noise

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

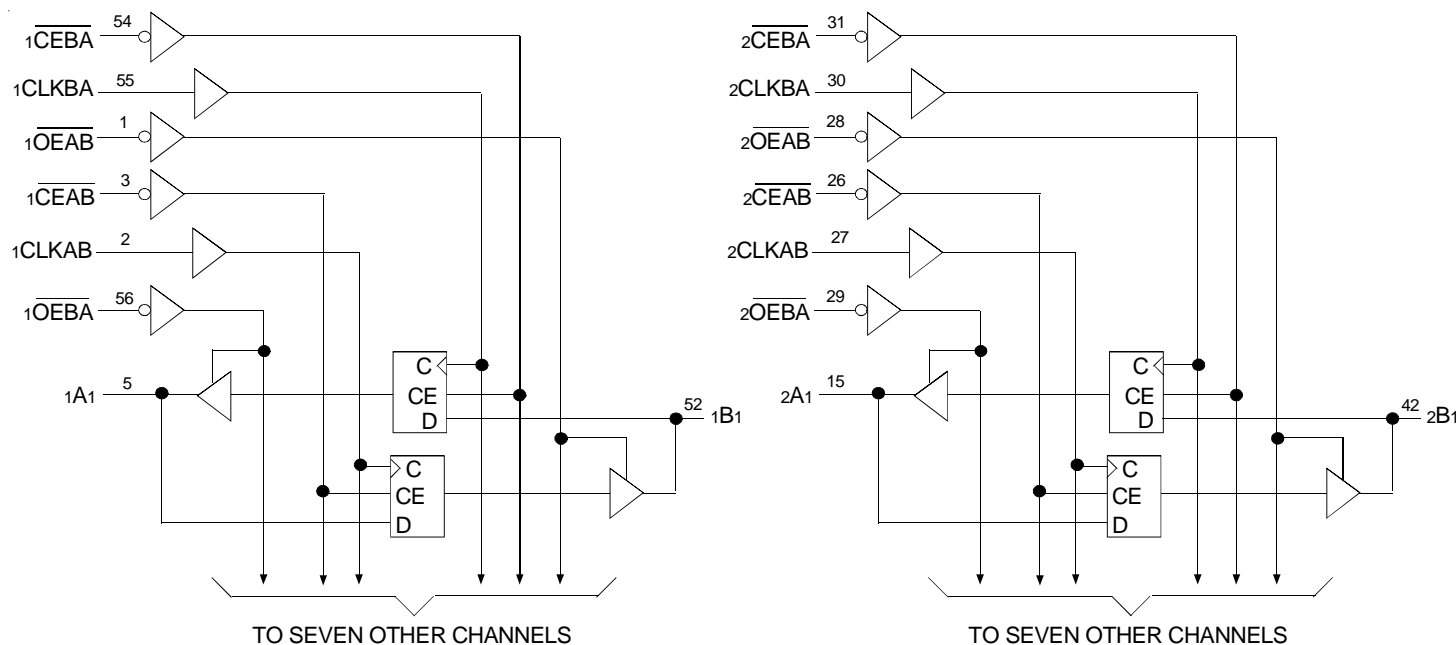
## DESCRIPTION:

This 16-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low power device is organized as two independent 8-bit D-type registered transceivers with separate input and output control for independent control of data flow in either direction. For example, the A-to-B Enable ( $\overline{CEAB}$ ) must be LOW to enter data from the A port. CLKAB controls the clocking function. When CLKAB toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register.  $\overline{OEAB}$  performs the output enable function on the B port. Data flow from the B port to A port is similar but requires using  $\overline{CEBA}$ , CLKBA, and  $\overline{OEBA}$  inputs. Full 16-bit operation is achieved by tying the control pins of the independent transceivers together.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

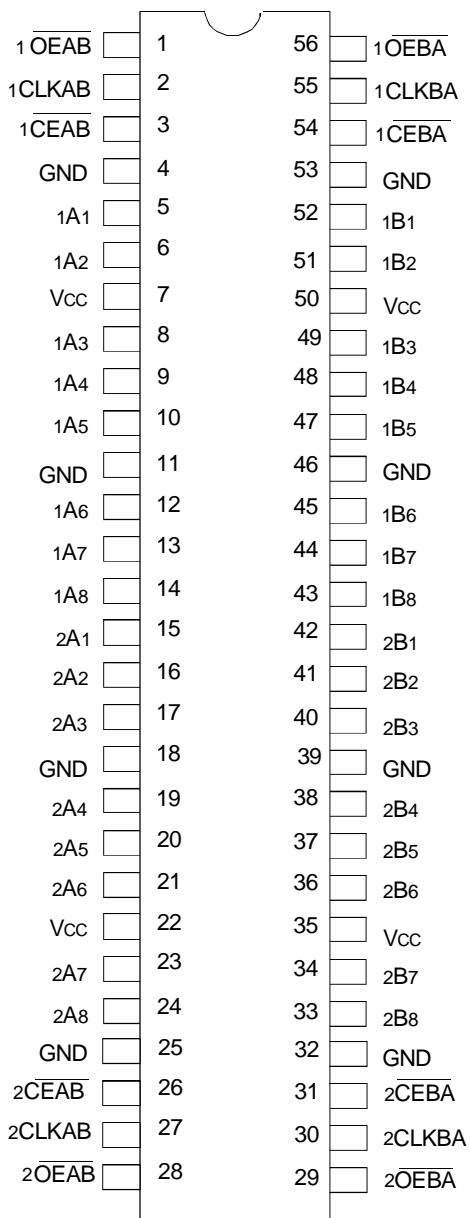
The LVCR162952A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been developed to drive  $\pm 12mA$  at the designated threshold levels.

## FUNCTIONAL BLOCK DIAGRAM



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## PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP  
TOP VIEW

## CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	6.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

**NOTE:**

1. As applicable to the device type.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## PIN DESCRIPTION

Pin Names	Description
x $\overline{OEAB}$	A-to-B Output Enable Inputs (Active LOW)
x $\overline{OEBA}$	B-to-A Output Enable Inputs (Active LOW)
x $\overline{CEAB}$	A-to-B Clock Enable Inputs (Active LOW)
x $\overline{CEBA}$	B-to-A Clock Enable Inputs (Active LOW)
xCLKAB	A-to-B Clock Inputs
xCLKBA	B-to-A Clock Inputs
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

## FUNCTION TABLE<sup>(1,2)</sup>

Inputs			Outputs	
x $\overline{CEAB}$	xCLKAB	x $\overline{OEAB}$	xAx	xBx
H	X	L	X	B <sup>(3)</sup>
X	L	L	X	B <sup>(3)</sup>
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

**NOTES:**

- A-to-B data flow is shown: B-to-A data flow is similar but uses x $\overline{CEBA}$ , xCLKBA, and x $\overline{OEBA}$ .
- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High Impedance  
↑ = LOW-to-HIGH Transition
- Output level of B before the indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		2	—	—	
$V_{IL}$	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		—	—	0.8	
$I_{IH}$ $I_{IL}$	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to $5.5\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$ $I_{OZL}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to $5.5\text{V}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 5.5\text{V}$		—	—	$\pm 50$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or $V_{CC}$	—	—	10	$\mu\text{A}$
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ , other inputs at $V_{CC}$ or GND		—	—	500	$\mu\text{A}$

### NOTES:

1. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
2. This applies in the disabled state only.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to $3.6\text{V}$	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -4\text{mA}$	1.9	—	
			$I_{OH} = -6\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$	$I_{OH} = -4\text{mA}$	2.2	—	
			$I_{OH} = -8\text{mA}$	2	—	
		$V_{CC} = 3\text{V}$	$I_{OH} = -6\text{mA}$	2.4	—	
$I_{OH} = -12\text{mA}$	2		—			
$V_{OL}$	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to $3.6\text{V}$	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 4\text{mA}$	—	0.4	
			$I_{OL} = 6\text{mA}$	—	0.55	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 4\text{mA}$	—	0.4	
			$I_{OL} = 8\text{mA}$	—	0.6	
		$V_{CC} = 3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.55	
$I_{OL} = 12\text{mA}$	—		0.8			

### NOTE:

1.  $V_{IH}$  and  $V_{IL}$  must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate  $V_{CC}$  range.  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

OPERATING CHARACTERISTICS,  $V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	$C_L = 0pF$ , $f = 10MHz$		pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled			

SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	2	7.6	2	6.6	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{xOEBA}$ , $\overline{xOEAB}$ to xAx, xBx	1.5	8	1.5	7	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{xOEBA}$ , $\overline{xOEAB}$ to xAx, xBx	1.5	7.5	1.5	6.5	ns
$t_{SU}$	Set-up Time, HIGH or LOW xAx, xBx before xCLKAB $\uparrow$ , xCLKBA $\uparrow$	2.5	—	2.5	—	ns
$t_H$	Hold Time, HIGH or LOW xAx, xBx after xCLKAB $\uparrow$ , xCLKBA $\uparrow$	1.5	—	1.5	—	ns
$t_{SU}$	Set-up Time, HIGH or LOW $\overline{xCEAB}$ , $\overline{xCEBA}$ before xCLKAB $\uparrow$ , xCLKBA $\uparrow$	1.8	—	1.4	—	ns
$t_H$	Hold Time, HIGH or LOW $\overline{xCEAB}$ , $\overline{xCEBA}$ after xCLKAB $\uparrow$ , xCLKBA $\uparrow$	2	—	2	—	ns
$t_W$	Pulse Width HIGH or LOW, xCLKAB or xCLKBA	3	—	3	—	ns
$t_{SK(0)}$	Output Skew <sup>(2)</sup>	—	—	—	500	ps

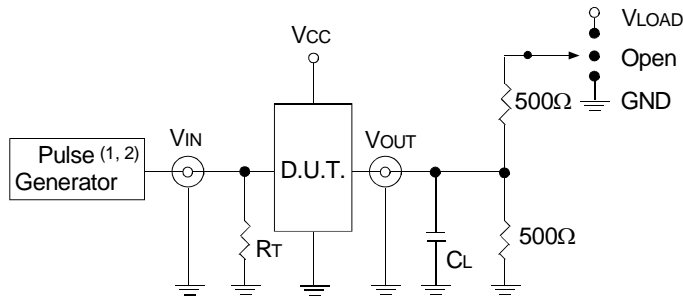
NOTES:

- See TEST CIRCUITS AND WAVEFORMS.  $T_A = -40^\circ C$  to  $+85^\circ C$ .
- Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> = 3.3V ± 0.3V	V <sub>CC</sub> <sup>(1)</sup> = 2.7V	V <sub>CC</sub> <sup>(2)</sup> = 2.5V ± 0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open

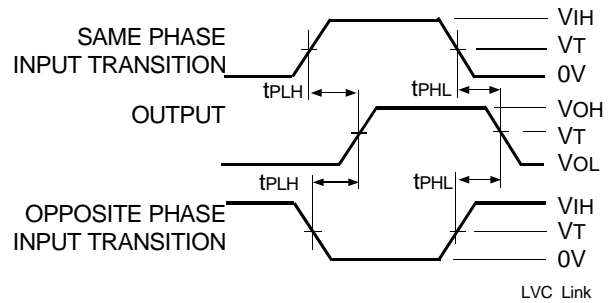


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

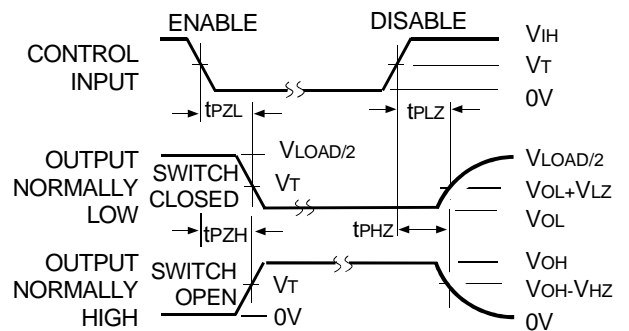
Output Skew - tsk(x)

#### NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



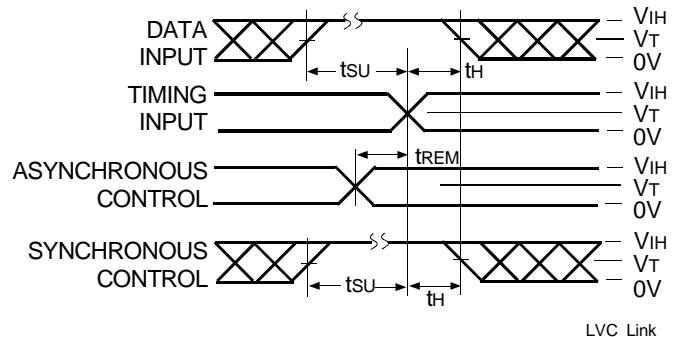
#### Propagation Delay



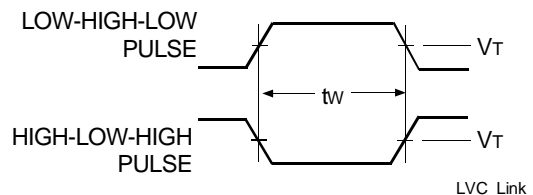
#### Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

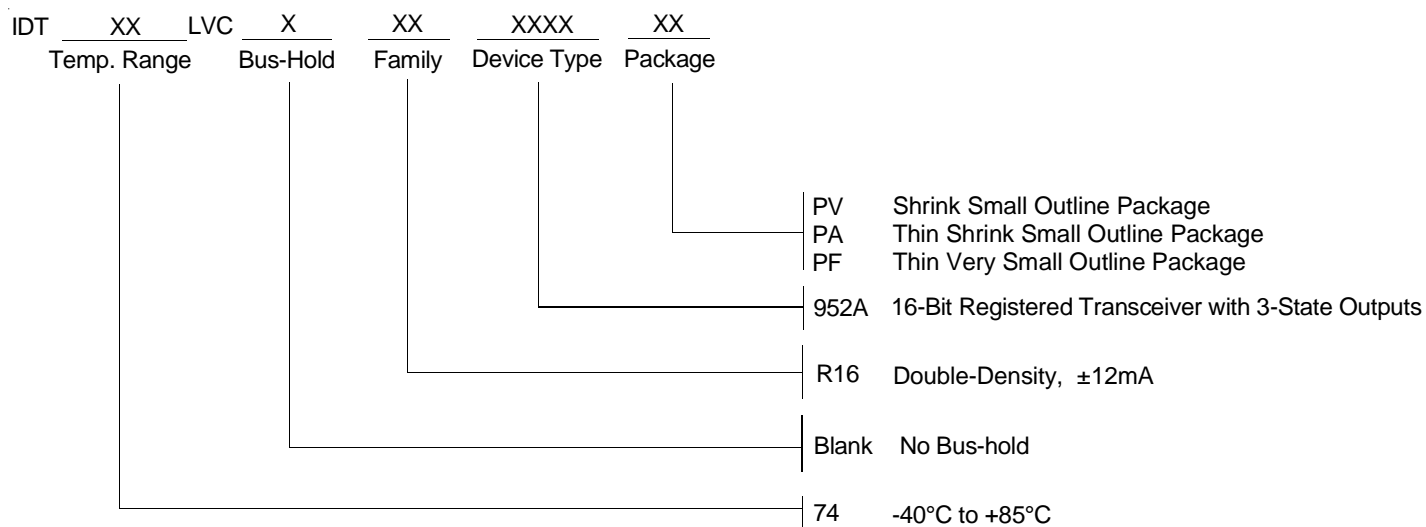


#### Set-up, Hold, and Release Times



#### Pulse Width

## ORDERING INFORMATION



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