QUAD 2-INPUT NAND GATE

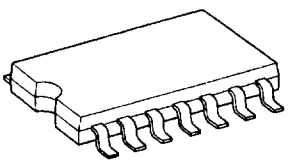
The TC74LVX00 is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C^2MOS technology. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low voltage and battery operated systems.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

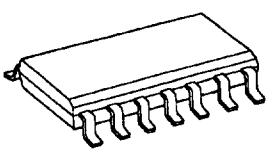
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

TC74LVX00F



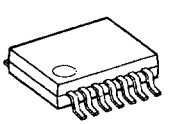
SOP14-P-300

TC74LVX00FN



SOL14-P-150

TC74LVX00FS



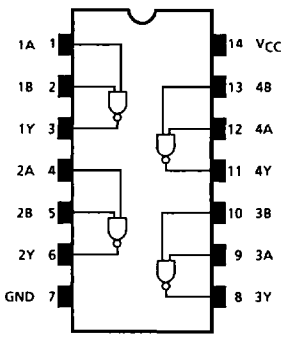
SSOP14-P-225

Weight SOP14-P-300 : 0.18g (Typ.)
SOL14-P-150 : 0.12g (Typ.)
SSOP14-P-225 : 0.07g (Typ.)

FEATURES

- High speed : $t_{pd} = 4.1ns$ (Typ.) ($V_{CC} = 3.3V$)
- Low power dissipation : $I_{CC} = 2\mu A$ (Max.) ($Ta = 25°C$)
- Input voltage level : $V_{IL} = 0.8V$ (Max.) ($V_{CC} = 3V$)
  $V_{IH} = 2.0V$ (Min.) ($V_{CC} = 3V$)
- Power down protection is provided on all inputs.
- Balanced propagation delays
  : $t_{pLH} \simeq t_{pHL}$
- Low noise : $V_{OLP} = 0.5V$ (Max.)
- Pin and function compatible with 74HC00

PIN ASSIGNMENT

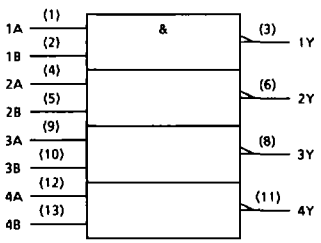


(TOP VIEW)

TRUTH TABLE

INPUT		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

IEC LOGIC SYMBOL



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C
Lead Temperature 10s	T_L	300	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Input Voltage	"H" Level	V_{IH}			2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	"L" Level	V_{IL}			2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	
				I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	
				I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
				I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
Input Leakage Current		I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.0	—	20.0	μA

AC characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	C_L (pF)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Propagation Delay Time	t_{pLH} t_{pHL}		2.7	15	—	5.4	10.1	1.0	12.5	ns
				50	—	7.9	13.6	1.0	16.0	
			3.3 ± 0.3	15	—	4.1	6.2	1.0	7.5	
				50	—	6.6	9.7	1.0	11.0	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	19	—	—	—	pF

(Note 1) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation :
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT