

CD4094BC 8-Bit Shift Register/Latch with 3-STATE Outputs

General Description

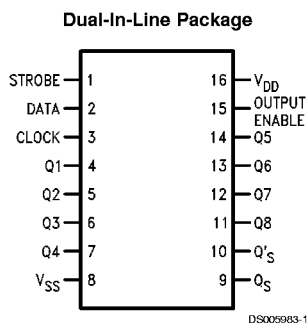
The CD4094BC consists of an 8-bit shift register and a 3-STATE 8-bit latch. Data is shifted serially through the shift register on the positive transition of the clock. The output of the last stage (Q_8) can be used to cascade several devices. Data on the Q_8 output is transferred to a second output, Q'_8 , on the following negative clock edge.

The output of each stage of the shift register feeds a latch, which latches data on the negative edge of the STROBE input. When STROBE is high, data propagates through the latch to 3-STATE output gates. These gates are enabled when OUTPUT ENABLE is taken high.

Features

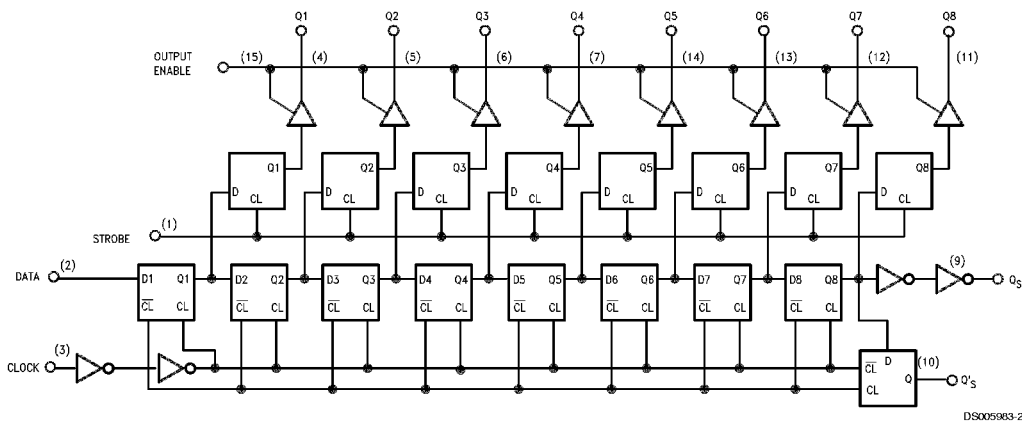
- Wide supply voltage range: 3.0V to 18V
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- 3-STATE outputs

Connection Diagram



Top View
Order Number CD4094B

Block or Logic Diagram



Absolute Maximum Ratings (Notes 2, 3)

(Soldering, 10 seconds)

260°C

Supply Voltage (V_{DD})	-0.5 to +18 V_{DC}
Input Voltage (V_{IN})	-0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	-65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	

Recommended Operating Conditions (Note 3)

DC Supply Voltage (V_{DD})	+3.0 to +15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	-40°C to +85°C

DC Electrical Characteristics

CD4094BC (Note 3)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent	$V_{DD} = 5.0V$		20			20		150	μA
	Device Current	$V_{DD} = 10V$		40			40		300	μA
		$V_{DD} = 15V$		80			80		600	μA
V_{OL}	Low Level	$V_{DD} = 5.0V$		0.05		0	0.05		0.05	V
	Output Voltage	$V_{DD} = 10V$ $ I_O \leq 1.0 \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level	$V_{DD} = 5.0V$	4.95		4.95	5.0		4.95		V
	Output Voltage	$V_{DD} = 10V$ $ I_O \leq 1 \mu A$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level	$V_{DD} = 5.0V, V_O = 0.5V$ or 4.5V		1.5			1.5		1.5	V
	Input Voltage	$V_{DD} = 10V, V_O = 1.0V$ or 9.0V		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level	$V_{DD} = 5.0V, V_O = 0.5V$ or 4.5V	3.5		3.5			3.5		V
	Input Voltage	$V_{DD} = 10V, V_O = 1.0V$ or 9.0V	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level	$V_{DD} = 5.0V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
	Output Current	$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level	$V_{DD} = 5.0V, V_O = 4.6V$	-0.52		-0.44	0.88		-0.36		mA
	Output Current	$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	2.25		-0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	-3.6		-3.0	8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3			-0.3		-1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.3			0.3		1.0	μA
I_{OZ}	3-STATE Output Leakage Current	$V_{DD} = 15V, V_{IN} = 0V$ or 15V		1			1		10	μA

AC Electrical Characteristics (Note 1)

$T_A = 25^\circ C, C_L = 50 pF$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Clock to Q_S	$V_{DD} = 5.0V$		300	600	ns
		$V_{DD} = 10V$		125	250	ns
		$V_{DD} = 15V$		95	190	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Q'_S	$V_{DD} = 5.0V$		230	460	ns
		$V_{DD} = 10V$		110	220	ns
		$V_{DD} = 15V$		75	150	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Parallel Out	$V_{DD} = 5.0V$		420	840	ns
		$V_{DD} = 10V$		195	390	ns
		$V_{DD} = 15V$		135	270	ns
t_{PHL}, t_{PLH}	Propagation Delay Strobe to Parallel Out	$V_{DD} = 5.0V$		290	580	ns
		$V_{DD} = 10V$		145	290	ns
		$V_{DD} = 15V$		100	200	ns
t_{PHZ}	Propagation Delay High	$V_{DD} = 5.0V$		140	280	ns

AC Electrical Characteristics (Note 1) (Continued)

$T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Level to High Impedance	$V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		75 55	150 110	ns ns
t_{PLZ}	Propagation Delay Low Level to High Impedance	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		140 75 55	280 150 110	ns ns ns
t_{PZH}	Propagation Delay High Impedance to High Level	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		140 75 55	280 150 110	ns ns ns
t_{PZL}	Propagation Delay High Impedance to Low Level	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		140 75 55	280 150 110	ns ns ns
t_{THL} , t_{TLH}	Transition Time	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 40	200 100 80	ns ns ns
t_{SU}	Set-Up Time Data to Clock	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	80 40 20	40 20 10		ns ns ns
t_r , t_f	Maximum Clock Rise and Fall Time	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	1 1 1			ms ms ms
t_{PC}	Minimum Clock Pulse Width	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	200 100 83	100 50 40		ns ns ns
t_{PS}	Minimum Strobe Pulse Width	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	200 80 70	100 40 35		ns ns ns
f_{max}	Maximum Clock Frequency	$V_{DD} = 5.0\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	1.5 3.0 4.0	3.0 6.0 8.0		MHz MHz MHz
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

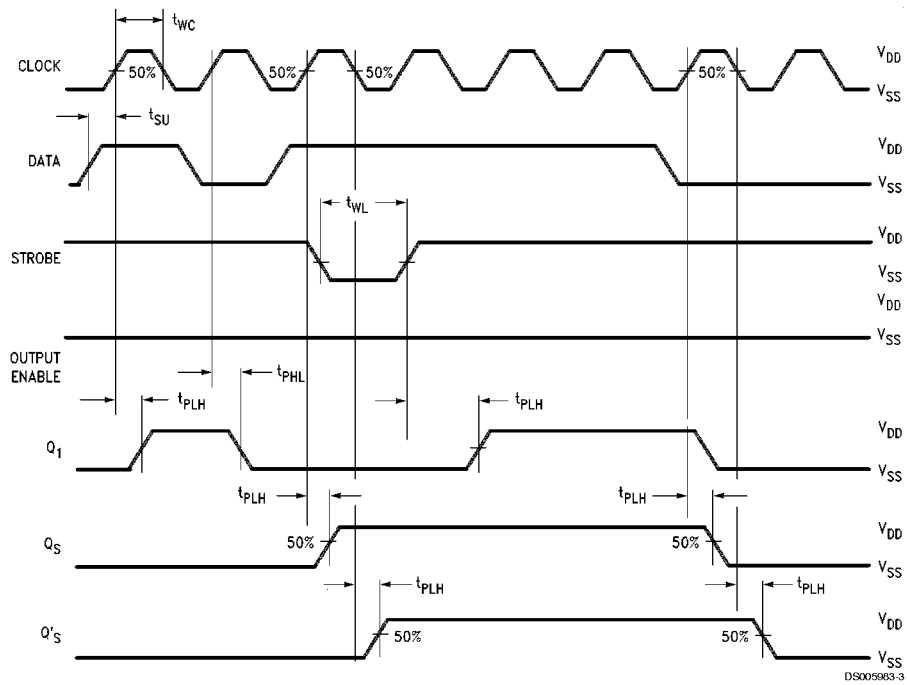
Note 1: AC Parameters are guaranteed by DC correlated testing.

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

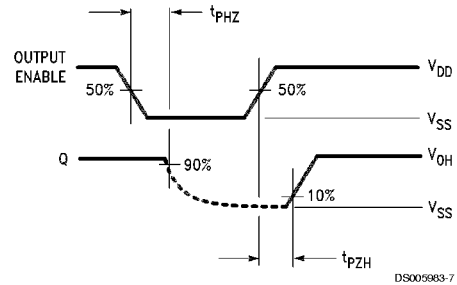
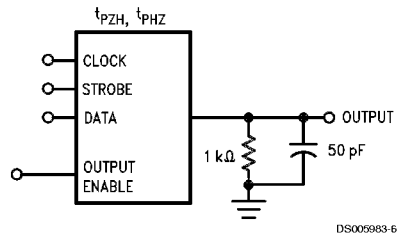
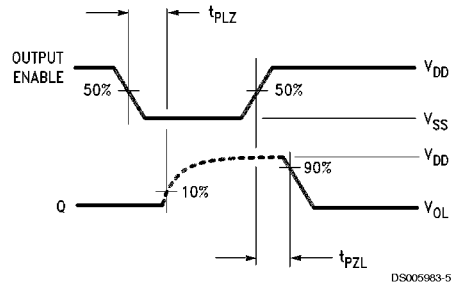
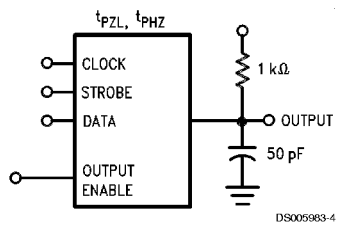
Note 3: $V_{SS} = 0\text{V}$ unless otherwise specified.

Note 4: I_{QH} and I_{QL} are tested one output at a time.

Timing Diagram



Test Circuits and Timing Diagrams for 3-STATE

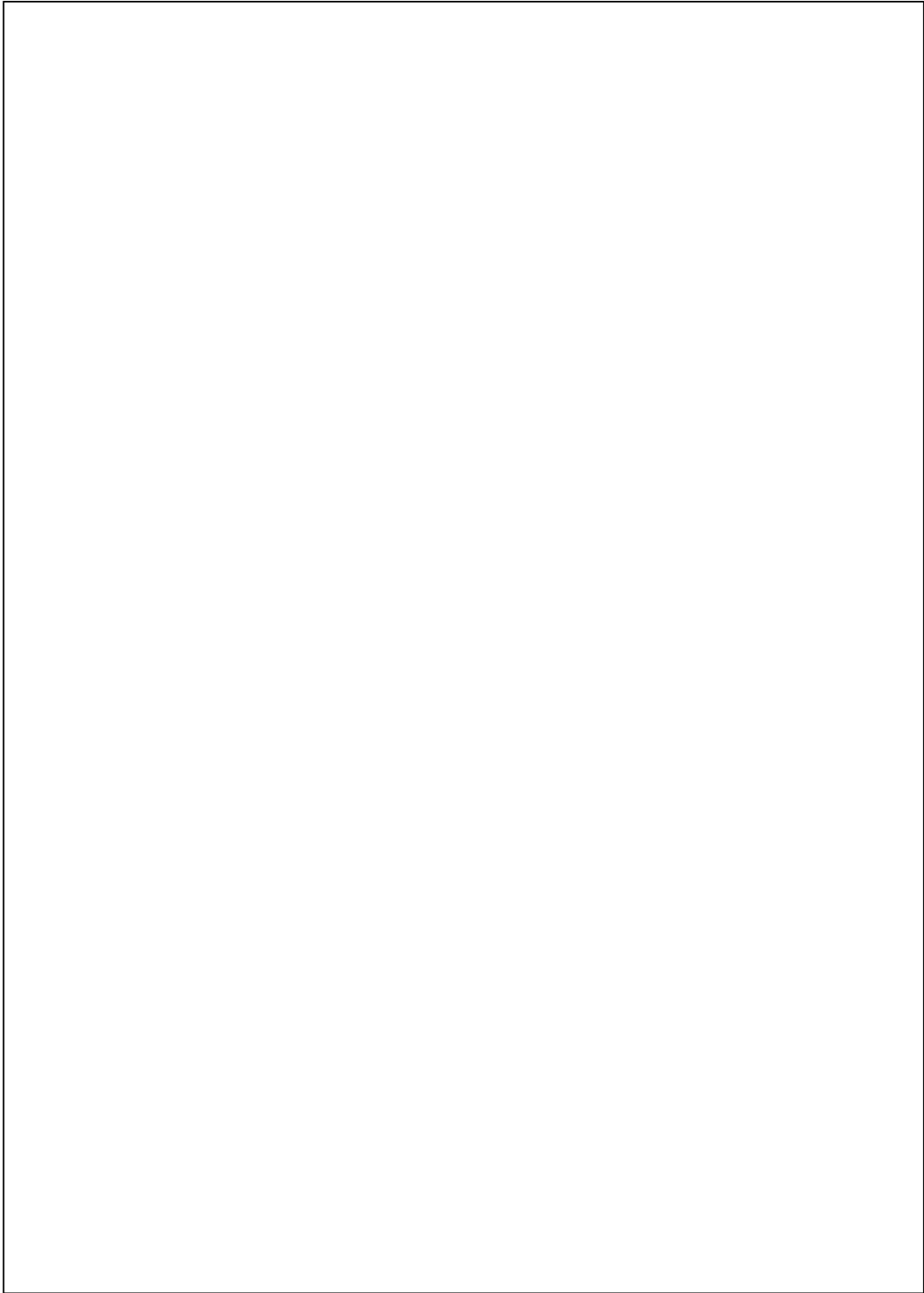


Logic Truth Table

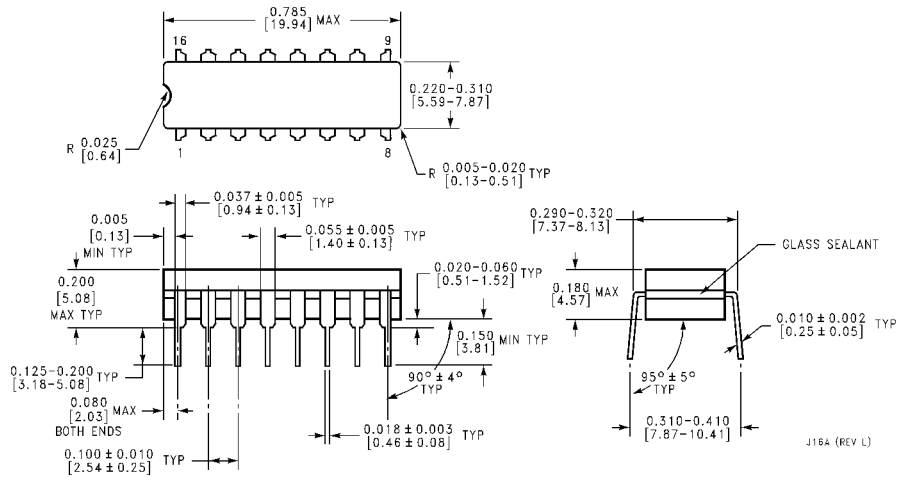
Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q _N	Q _S *	Q' _S
⎯	0	X	X	Hi-Z	Hi-Z	Q7	No Chg.
⎯	0	X	X	Hi-Z	Hi-Z	No Chg.	Q7
⎯	1	0	X	No Chg.	No Chg.	Q7	No Chg.
⎯	1	1	0	0	Q _N -1	Q7	No Chg.
⎯	1	1	1	1	Q _N -1	Q7	No Chg.
⎯	1	1	1	No Chg.	No Chg.	No Chg.	Q7

X = Don't Care

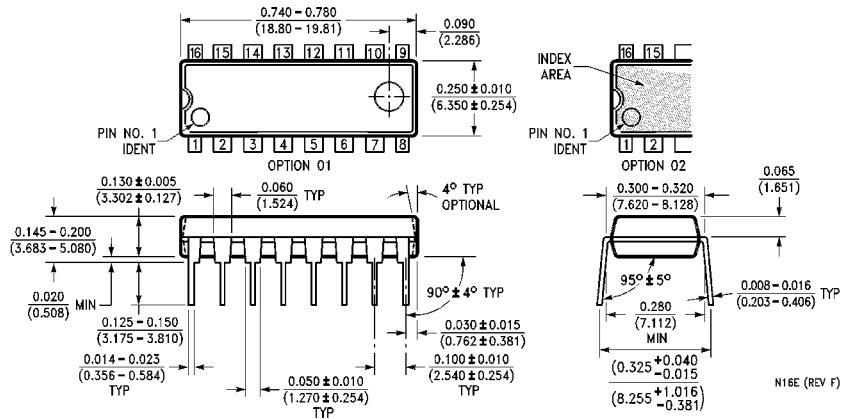
*At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.



Physical Dimensions inches (millimeters) unless otherwise noted



Order Number CD4094BCJ
Package Number J16A



Order Number CD4094BCN
Package Number N16E