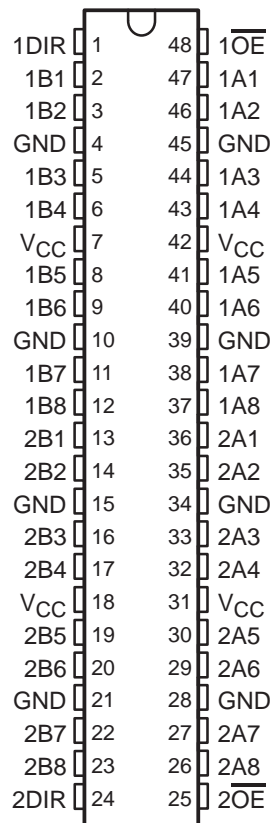


SN54LVTH16245A, SN74LVTH16245B 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS143M – MAY 1992 – REVISED MARCH 2000

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II (SN74LVTH16245B Only)
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101) (SN74LVTH16245B Only)
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16245A . . . WD PACKAGE
SN74LVTH16245B . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The SN54LVTH16245A and SN74LVTH16245B devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so that the buses are effectively isolated.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH16245A, SN74LVTH16245B 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS143M – MAY 1992 – REVISED MARCH 2000

description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH16245A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16245B is characterized for operation from -40°C to 85°C .

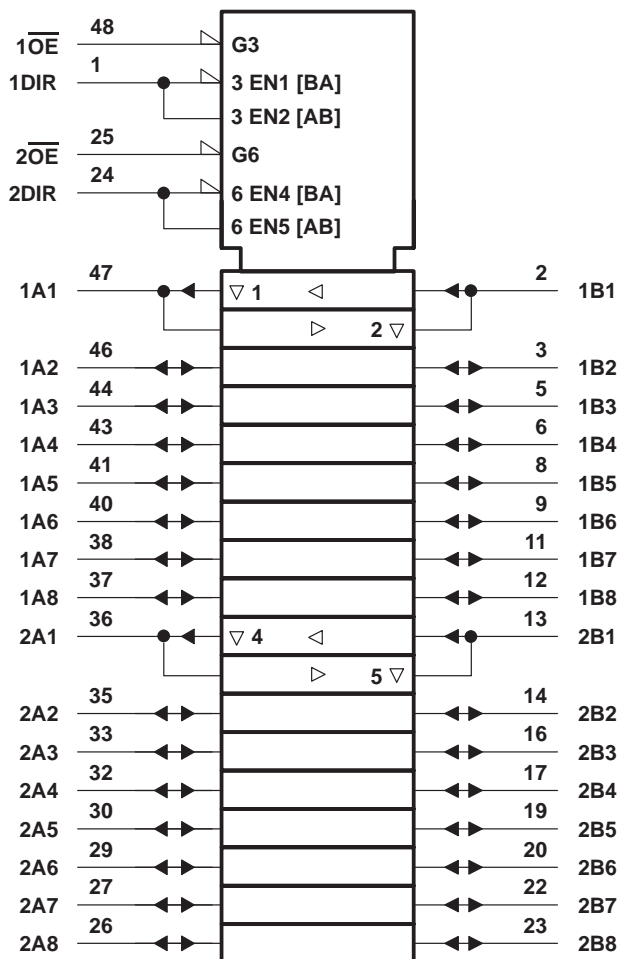
FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN54LVTH16245A, SN74LVTH16245B
 3.3-V ABT 16-BIT BUS TRANSCEIVERS
 WITH 3-STATE OUTPUTS

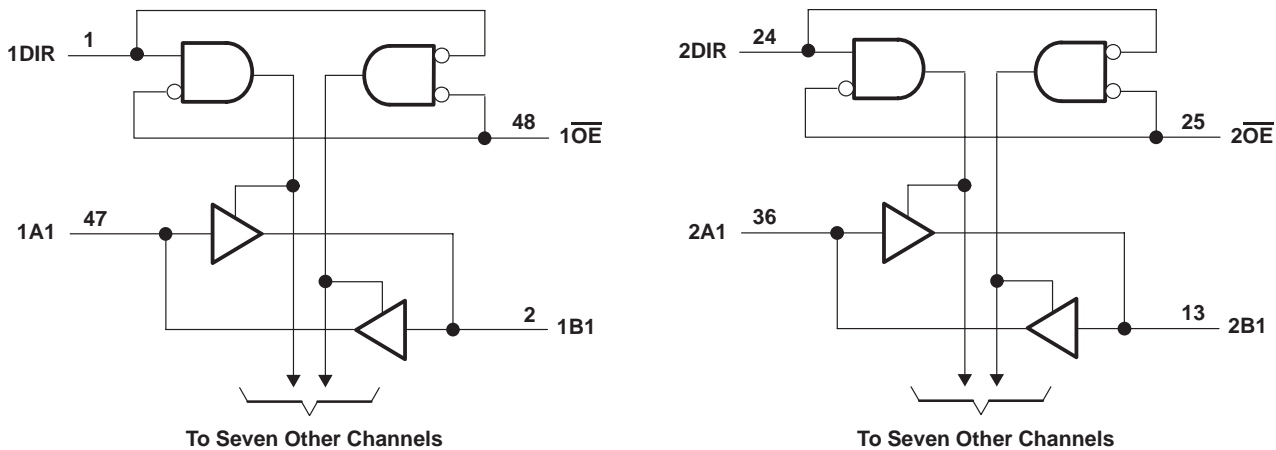
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH16245A, SN74LVTH16245B

3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS143M – MAY 1992 – REVISED MARCH 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16245A	96 mA
SN74LVTH16245B	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16245A	48 mA
SN74LVTH16245B	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

	SN54LVTH16245A		SN74LVTH16245B		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage		5.5		5.5	V
I_{OH} High-level output current		–24		–32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate	200		200		μs/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVTH16245A, SN74LVTH16245B 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVTH16245A			SN74LVTH16245B			UNIT		
			MIN	TYP†	MAX	MIN	TYP†	MAX			
V_{IK}		$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$	-1.2			-1.2			V		
V_{OH}		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V		
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4					
		$V_{CC} = 3\text{ V}$	2			2					
V_{OL}		$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$	0.2			0.2			V	
			$I_{OL} = 24\text{ mA}$	0.5			0.5				
		$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$	0.4			0.4				
			$I_{OL} = 32\text{ mA}$	0.5			0.5				
			$I_{OL} = 48\text{ mA}$	0.55			0.55				
			$I_{OL} = 64\text{ mA}$	0.55			0.55				
I_I		Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$	± 1			± 1			μA	
			$V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$	10			10				
		A or B ports‡	$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V}$	20			20			
				$V_I = V_{CC}$	5			1			
			$V_I = 0$	-5			-5				
I_{off}		$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				± 100			μA		
$I_I(\text{hold})$		A or B ports	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	75			75			μA
				$V_I = 2\text{ V}$	-75			-75			
		$V_{CC} = 3.6\text{ V}\S$, $V_I = 0\text{ to }3.6\text{ V}$				± 500					
I_{OZPU}		$V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$	$\pm 100^*$			± 100			μA		
I_{OZPD}		$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$	$\pm 100^*$			± 100			μA		
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high	0.19			0.19			mA	
			Outputs low	5			5				
			Outputs disabled	0.19			0.19				
$\Delta I_{CC}\P$		$V_{CC} = 3\text{ V to }3.6$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$	0.2			0.2			mA		
C_i		$V_I = 3\text{ V or }0$	4			4			pF		
C_{io}		$V_O = 3\text{ V or }0$	10			10			pF		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at V_{CC} or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54LVTH16245A, SN74LVTH16245B
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS143M – MAY 1992 – REVISED MARCH 2000

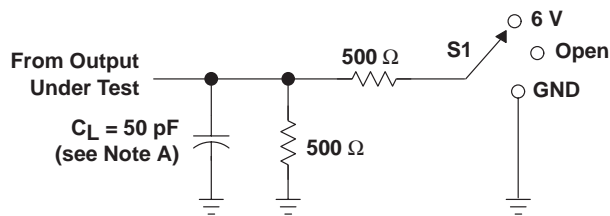
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16245A				SN74LVTH16245B				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t_{PLH}	A or B	B or A	0.5	4.5	4.6		1.5	2.3	3.3	3.7		ns
t_{PHL}			0.5	4.4	3.9		1.3	2.1	3.3	3.5		
t_{PZH}	\overline{OE}	A or B	0.5	6.5	6.6		1.5	2.8	4.5	5.3		ns
t_{PZL}			0.5	5.4	6.2		1.6	2.9	4.6	5.2		
t_{PHZ}	\overline{OE}	A or B	1	6.8	7		2.3	3.7	5.1	5.5		ns
t_{PLZ}			1	6.2	6.3		2.2	3.5	5.1	5.4		
$t_{sk(o)}$								0.5			ns	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

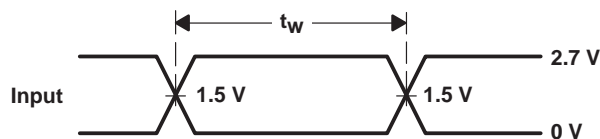


PARAMETER MEASUREMENT INFORMATION

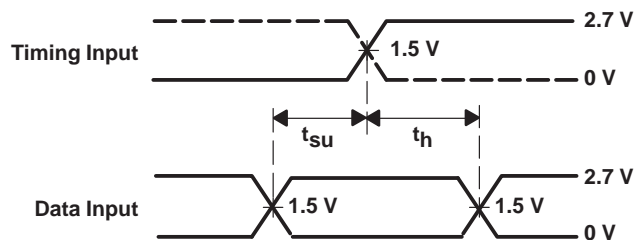


LOAD CIRCUIT

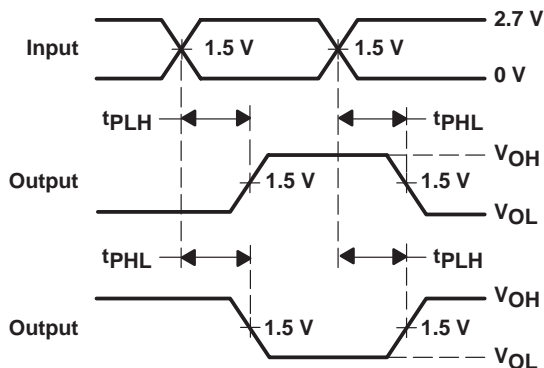
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



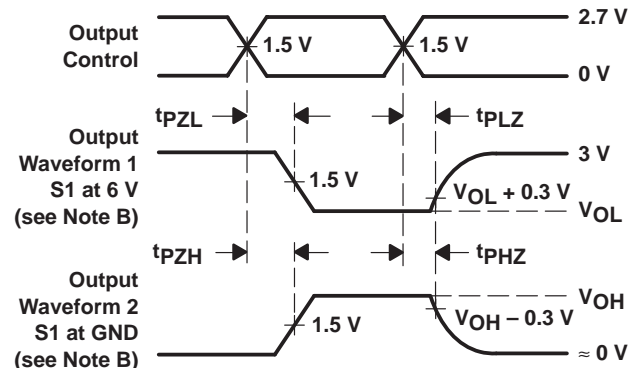
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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SN54LVTH16245A, 3.3-V ABT 16-Bit Bus Transceivers With 3-State Outputs

Device Status: Active

- > [Description](#)
- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)
- > [Related Documents](#)
- > [Training](#)

Parameter Name	SN54LVTH16245A
Voltage Nodes (V)	3.3, 2.7
Vcc range (V)	2.7 to 3.6
Input Level	TTL/CMOS
Output Level	LVTTL
No. of Outputs	16
Logic	True

Description

The SN54LVTH16245A and SN74LVTH16245B devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

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Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, OE \setminus should be

connected to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

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Features

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To view the following documents, [Acrobat Reader 3.x](#) is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: [scbs143m.pdf](#) (110 KB)

Full datasheet in Zipped PostScript: [scbs143m.psz](#) (113 KB)

Pricing/Samples/Availability

<u>Orderable Device</u>	<u>Package</u>	<u>Pins</u>	<u>Temp (°C)</u>	<u>Status</u>	<u>Price/unit USD (100-999)</u>	<u>Pack Qty</u>	<u>DSCC Number</u>	<u>Availability / Samples</u>
5962-9668601QXA	WD	48	-55 TO 125	ACTIVE	24.22	1		Check stock or order
SNJ54LVTH16245AWD	WD	48	-55 TO 125	ACTIVE	24.22	1		Check stock or order

Application Reports

View Application Reports for [Digital Logic](#)

- [Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs](#) (SCBA012A - Updated: 08/01/1997)
- [Implications Of Slow Or Floating CMOS Inputs](#) (SCBA004C - Updated: 02/01/1998)
- [Input And Output Characteristics Of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [LVT Family Characteristics](#) (SCEA002A - Updated: 03/01/1998)
- [LVT-to-LVTH Conversion](#) (SCEA010 - Updated: 12/08/1998)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Logic Solutions For IEEE Std 1284](#) (SCEA013 - Updated: 06/01/1999)
- [Mixed 3.3-V And 5-V Systems With LVT Logic](#) (SCBA005 - Updated: 04/01/1993)
- [Understanding Advanced Bus-Interface Products Design Guide](#) (SCAA029, 253 KB - Updated: 05/01/1996)

Related Documents

- [Documentation Rules \(SAP\) And Ordering Information](#) (SZZU001B, 4 KB - Updated: 05/06/1999)
- [Logic Selection Guide Second Half 2000](#) (SDYU001N, 5035 KB - Updated: 04/17/2000)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 284 KB - Updated: 07/28/2000)
- [More Power In Less Space - Technical Article](#) (SCAU001A, 850 KB - Updated: 03/01/1996)

Table Data Updated on: 9/7/2000