

ICS8304-01

Low Skew, 1-TO-4

LVCMOS / LVTTL INVERTING FANOUT BUFFER

GENERAL DESCRIPTION



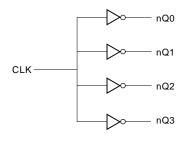
The ICS8304-01 is a low skew, 1-to-4 Inverting Fanout Bufferand a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8304-01 is characterized at full 3.3V for input VDD,

and mixed 3.3V and 2.5V for output operating supply modes (VDDO). Guaranteed output and part-to-part skew characteristics make the ICS8304-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

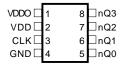
FEATURES

- 4 LVCMOS / LVTTL outputs
- Output frequency up to 166MHz
- · LVCMOS clock input
- 3.3V input, outputs may be either 3.3V or 2.5V supply modes
- Small 8 lead SOIC package saves board space
- 0°C to 70°C ambient operating temperature
- Industrial temperature version available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8304-01

8-Lead SOIC
3.8mm x 4.8mm x 1.47mm package body
M Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



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TABLE 1. PIN DESCRIPTIONS

Number	Name	Туре		Description	
1	VDDO	Power		Power supply pin. Connect to 3.3V or 2.5V.	
2	VDD	Power		Power supply pin. Connect to 3.3V.	
3	CLK	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.	
4	GND	Power		Power supply ground. Connect to ground.	
5	nQ3	Output		Inverted version of clock input. LVCMOS / LVTTL interface levels.	
6	nQ2	Output		Inverted version of clock input. LVCMOS / LVTTL interface levels.	
7	nQ1	Output		Inverted version of clock input. LVCMOS / LVTTL interface levels.	
8	nQ0	Output		Inverted version of clock input. LVCMOS / LVTTL interface levels.	

NOTE: Pullup and Pulldown refers to internal input resistors. See Table 2, Pin Characterisicts, for typical value.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	CLK				4	pF
CPD	Power Dissipation Capacitance				TBD		pF
RPULLUP	Input Pullup Resisto	r			51		ΚΩ
RPULLDOWN	Input Pulldown Resistor				51		ΚΩ
ROUT	Output Impedance						Ω



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx} 4.6V

 $\begin{array}{lll} \text{Inputs, V}_{\text{I}} & & -0.5 \text{V to V}_{\text{DD}} + 0.5 \text{V} \\ \text{Outputs, V}_{\text{O}} & & -0.5 \text{V to V}_{\text{DDO}} + 0.5 \text{V} \\ \end{array}$

Package Thermal Impedance, θ_{JA} 112°C/W Storage Temperature, T_{STG} -65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, VDD = VDDO = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD	Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		3.135	3.3	3.465	V
GND	Power Supply Current				50	mA

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS, VDD = VDDO = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	CLK		2		3.765	V
VIL	Input Low Voltage	CLK		-0.3		0.8	V
IIH	Input High Current	CLK				150	μΑ
IIL	Input Low Current	CLK		-5			μΑ
VOH	Output High Voltage						V
VOL	Output Low Voltage						V

TABLE 3C. Power Supply DC CHARACTERISTICS, VDD = 3.3V±5%, VDDO = 2.5V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD	Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		2.375	2.5	2.625	V
GND	Power Supply Current				50	mA

TABLE 3D. LVCMOS / LVTTL DC CHARACTERISTICS, VDD = 3.3V±5%, VDDO = 2.5V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	CLK		2		3.765	V
VIL	Input Low Voltage	CLK		-0.3		0.8	V
IIH	Input High Current	CLK				150	μΑ
IIL	Input Low Current	CLK		-5			μΑ
VOH	Output High Voltage						V
VOL	Output Low Voltage						V

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ICS8304-01

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Table 4. AC Characteristics, VDD = 3.3V±5%, VDDO = 2.5V±5%, Ta=0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				166	MHz
tpLH	Propagation Delay, Low-to-High; NOTE 1		2.1		3.9	ns
tpHL	Propagation Delay, High-to-Low; NOTE 1					ns
tsk(o)	Output Skew; NOTE 2			30	52	ps
tsk(pp)	Part-to-Part; NOTE 3				250	ps
tR	Output Rise Time	30% to 70%		670		ps
tF	Output Fall Time	30% to 70%		900		ps
tPW	Output Pulse Width	f = 166MHz	2.5		3.3	ns
I LE VV	Output Fuise Width	$0Hz \le f \le 166MHz$	tcycle/2 - 700	tcycle/2	tcycle/2 + 700	ps
tEN	Output Enable Time; NOTE 4					ns
tDIS	Output Disable Time; NOTE 4					ns
tS	Clock Enable Setup Time					ns
tH	Clock Enable Hold Time					ns

All parameters measured at 166MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: Measured by triggering on input signal and measuring the largest displacement between output cycles.

ICS8304-01

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PACKAGE OUTLINE - SUFFIX M

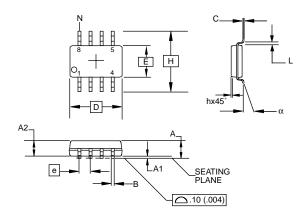


TABLE 5. PACKAGE DIMENSIONS

SYMBOL	Millin	neters	Inches			
STWIBOL	MINIMUN	MAXIMUM	MINIMUN	MAXIMUM		
N		8				
А	1.35	1.75	0.532	0.0688		
A1	0.10	0.25	0.0040	0.0098		
В	0.33	0.51	0.013	0.020		
С	0.19	0.25	0.0075	0.0098		
D	4.80	5.00	0.1890	0.1968		
E	3.80	4.00	0.1497	0.1574		
е	1.27 E	BASIC	0.050	BASIC		
Н	5.80	6.20	0.2284	0.2440		
h	0.25	0.50	0.010	0.020		
L	0.40	1.27	0.016	0.050		
α	0°	8°	0°	8°		

Reference Document: JEDEC Publication 95, MS-013, MO-119



ICS8304-01

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TABLE 6. ORDERING INFORMATION

Part/Order Number	Marking	Marking Package		Temperature
ICS8304G-01	ICS4A01	8 lead TSSOP	100 per tube	0°C to 70°C
ICS8304G-01T	ICS4A01	8 lead TSSOP on Tape and Reel	2500	0°C to 70°C
ICS8304M-01	ICS8304-01	8 lead SOIC	96 per tube	0°C to 70°C
ICS8304M-01T	ICS8304-01	8 lead SOIC on Tape and Reel	2500	0°C to 70°C

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