PERICOM

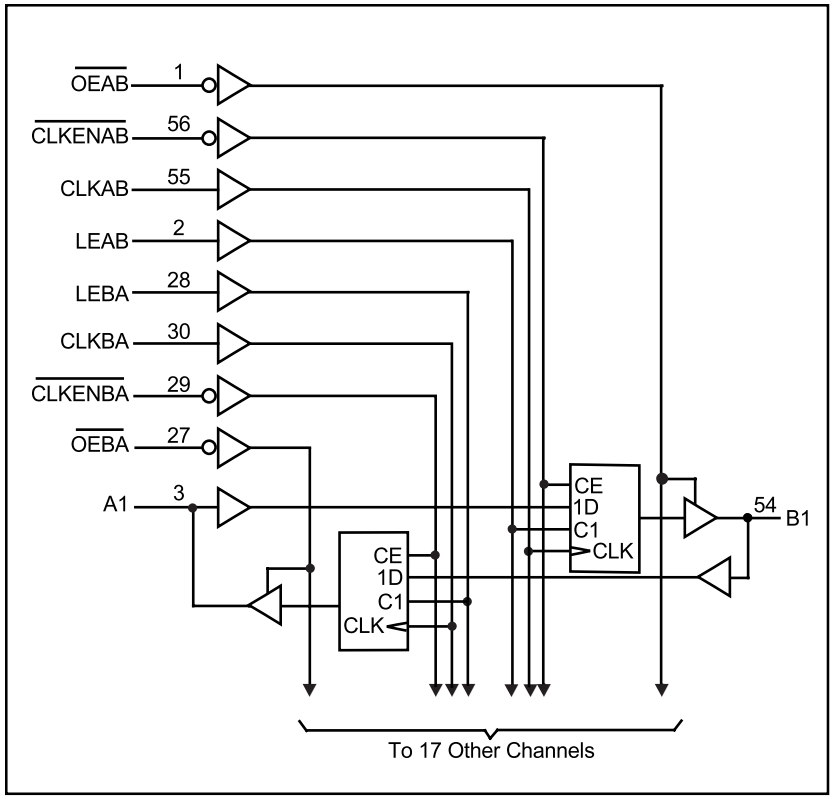
PI74AVC16601
PI74AVCH16601

18-Bit Universal Bus Transceiver With 3-State Outputs

Product Features

- Designed for low voltage operation, V_{CC} = 1.65V to 3.6V
- Sub 2.0ns delays at 2.5V and 3.3V
- Dynamic Impedance Control on outputs, current drive > ±24mA at 2.5V_{CC}
- Patented noise reduction circuit
- I/O Tolerant to 3.6V, Inputs and Outputs for mixed voltage systems
- Supports live insertion
- Industrial operation at -40°C to +85°C
- Available Packages:
  – 48-pin 240 mil wide plastic TSSOP (A48)
  – 48-pin 173 mil wide plastic TVSOP (K48)

Logic Block Diagram



Product Description

Pericom Semiconductor's PI74AVC series of logic circuits are produced using the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

The function uses D-type latches and D-type flip-flops with 3-state outputs to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by Output Enable ($\overline{OEAB}$ and $\overline{OEBA}$), Latched Enable (LEAB and LEBA), and Clock (CLKAB and CLKBA) inputs. The clock can be controlled by the Clock Enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is HIGH, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

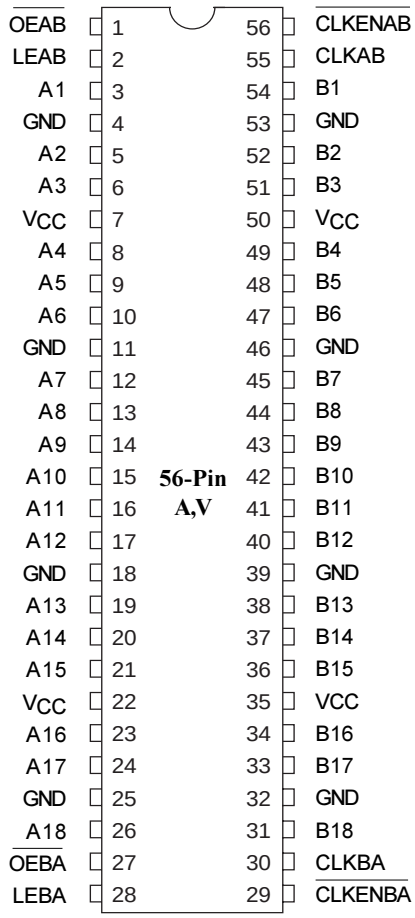
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The PI74AVCH16601 has "Bus Hold" which retains the data input's last state whenever the data input goes to high-impedance preventing "floating" inputs and eliminating the need for pullup/down resistors.

Product Pin Description

Pin Name	Description
$\overline{CLKEN}$	Clock Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable (Active HIGH)
CLK	Clock Input (Active HIGH)
Ax	Data I/O
Bx	Data I/O
GND	Ground
VCC	Power

Product Pin Configuration



Truth Table(1)†

Inputs					Output B
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

Notes:

1. H = High Signal Level
   L = Low Signal Level
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB is HIGH before LEAB goes LOW.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Applied ..... –10°C to +85°C
Input Voltage Range, V_{IN} ..... –0.5V to V_{CC} + 0.5V
Output Voltage Range, V_{OUT} ..... –0.5V to V_{CC} + 0.5V
DC Input Voltage ..... –0.5V to + 0.5V
DC Output Current 100mA
Power Dissipation 1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions(1)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 2.7V to 3.6V	2.0			
V_{IL}	Input LOW Voltage	V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 2.7V to 3.6V			0.8	
V_{IN}	Input Voltage		0		V_{CC}	
V_{OUT}	Output Voltage		0		V_{CC}	
I_{OH}	High-level Output Current	V_{CC} = 2.3V			-12	mA
		V_{CC} = 2.7V			-12	
		V_{CC} = 3.0V			-24	
I_{OL}	Low-level Output Current	V_{CC} = 2.3V			12	
		V_{CC} = 2.7V			12	
		V_{CC} = 3.0V			24	
T_A	Operating Free-Air Temperature		-40		85	°C

Note: Unused control inputs must be held HIGH or LOW to prevent them from floating.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ± 10%)

Parameters	Test Conditions		V_{CC}[1]	Min.	Typ.[2]	Max.	Units
V_{OH}	I_{OH} = -100µA		Min. to Max.	V_{CC} -0.2			V
	I_{OH} = -6mA	V_{IH} = 1.7V	2.3V	2.0			
	I_{OH} = -12mA	V_{IH} = 1.7V	2.3V	1.7			
		V_{IH} = 2.0V	2.7V	2.2			
		V_{IH} = 2.0V	3.0V	2.4			
	I_{OH} = -24mA	V_{IH} = 2.0V	3.0V	2.0			
V_{OL}	I_{OH} = -100µA		Min. to Max.	V_{CC} -0.2		0.2	
	I_{OH} = 6mA	V_{IH} = 0.7V	2.3V			0.4	
	I_{OH} = 12mA	V_{IH} = 0.7V	2.3V			0.7	
		V_{IH} = 0.8V	2.7V			0.4	
	I_{OH} = 24mA	V_{IH} = 0.8V	3.0V			0.55	
I_I	V_I = V_{CC} or GND		3.6V			±5	µA
I_I (Hold)[3]	V_I = 0.7V		2.3V	45			
	V_I = 1.7V			-45			
	V_I = 0.8V		3.0V	75			
	V_I = 2.0V			-75			
	V_I = 0 to 3.6V		3.6V			±500	
I_{OZ}[4]	V_O = V_{CC}or GND		3.6V			±10	
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6V			40	
ΔI_{CC}	One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND		3V to 3.6V			750	
C_I Control Inputs	V_I = V_{CC} or GND		3.3V		4		pF
C_{IO} A or B ports	V_O = V_{CC} or GND		3.3V		8		

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. Bus Hold maximum dynamic current required to switch the input from one state to another.
4. For I/O ports, the I_{OZ} includes the input leakage current.

Timing Requirements over Operating Range

Parameters	Description	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock frequency	0	150	0	150	0	150	MHz
t_W Pulse Duration	LE high	3.3		3.3		3.3		ns
	CLK high or low	3.3		3.3		3.3		
t_{SU} Setup time	Data before CLK high	2.3		2.4		2.1		
	Data before LE low, CLK high	2.0		1.6		1.6		
	Data before LE low, CLK low	1.3		1.2		1.1		
	$\overline{CLKEN}$ before CLK high	2.0		2.0		1.7		
t_H Hold time	Data after CLK high	0.7		0.7		0.8		
	Data after LE low, CLK high	1.3		1.6		1.4		
	Data after LE low, CLK low	1.7		2.0		1.7		
	$\overline{CLKEN}$ after CLK high	0.3		0.5		0.6		
$\Delta t/\Delta v$(1)	Input Transition Rise or Fall	0	10	0	10	0	10	ns/V

Note: Unused control inputs must be held HIGH or LOW to prevent them from floating.

Switching Characteristics over Operating Range[1]

Parameters	From (INPUT)	To (OUTPUT)	V_{CC} = 2.5V ±0.2V		V_{CC} = 2.7V		V_{CC} = 3.3 V ± 0.3V		Units
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
f_{MAX}			150		150		150		MHz
t_{PD}	A or B	B or A	1.3	4.9		4.6	1	4.1	ns
t_{PD}	LEBA or LEBA	A or B	1.2	5.6		5.3	1	4.7	
t_{PD}	CLKAB or CLKBA		1.7	6.2		5.8	1.4	5	
t_{EN}	$\overline{OEAB}$ or $\overline{OEBA}$		1.2	6.1		6.1	1.1	5.2	
t_{DIS}	$\overline{OEAB}$ or $\overline{OEBA}$		2.1	5.4		4.8	1.6	4.4	

Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Operating Characteristics, $T_A = 25^oC$

Parameter		Test Conditions	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Units
			Typical		
C_{PD} Power Dissipation Capacitance	Outputs Enabled	C_L = 50pF, f = 10 MHz	41	52	pF
	Outputs Disabled		6	6	