MOTOROLA

Military 54ALS573

Octal D-Type Transparent Latch With 3-State Outputs

ELECTRICALLY TESTED PER:
MPG54ALS573

AVAILABLE AS:

1) JAN: N/A
2) SMD: 8401201
3) 883C: 54ALS573/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2
***Call Factory for latest update**

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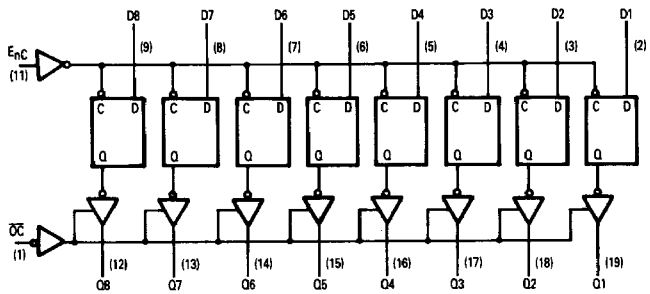
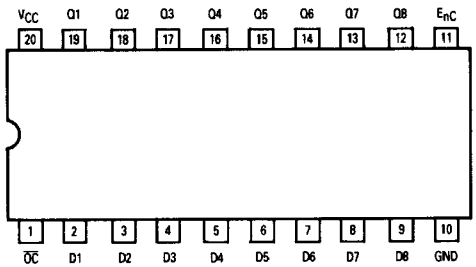
LOGIC DIAGRAM



CONNECTION DIAGRAM

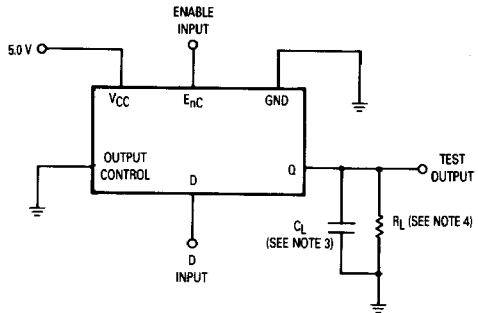


PIN ASSIGNMENTS

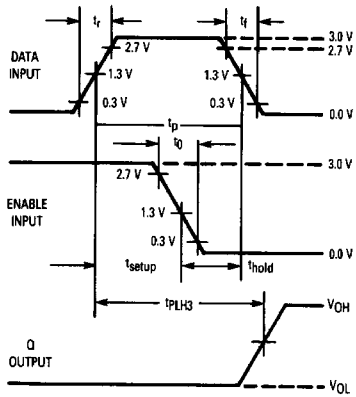
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{OC}$	1	1	1	V_{CC}
D1	2	2	2	V_{CC}
D2	3	3	3	V_{CC}
D3	4	4	4	V_{CC}
D4	5	5	5	V_{CC}
D5	6	6	6	V_{CC}
D6	7	7	7	V_{CC}
D7	8	8	8	V_{CC}
D8	9	9	9	V_{CC}
GND	10	10	10	GND
E_{nC}	11	11	11	V_{CC}
Q8	12	12	12	OPEN
Q7	13	13	13	OPEN
Q6	14	14	14	OPEN
Q5	15	15	15	OPEN
Q4	16	16	16	OPEN
Q3	17	17	17	OPEN
Q2	18	18	18	OPEN
Q1	19	19	19	OPEN
V_{CC}	20	20	20	V_{CC}

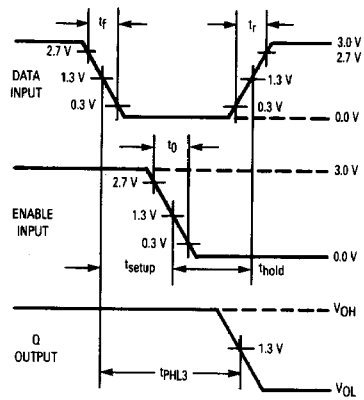
BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

DATA SWITCHING TEST CIRCUIT AND WAVEFORMS

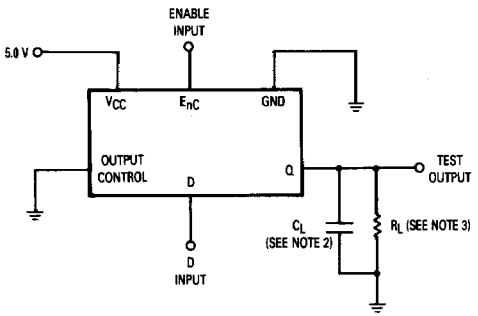


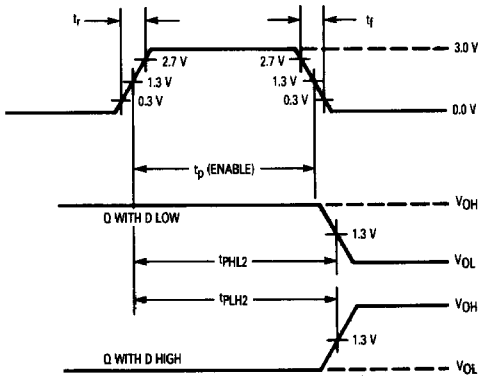
NOTES:
1. Enable input pulse characteristics: t_f = 6.0 ± 1.5 ns, t_p = 10 ns, PRR ≤ 1.0 MHz and Z_{out} ≈ 50 Ω.
2. D input pulse characteristics: t_r = t_f = 6.0 ± 1.5 ns, t_{setup} = 10 ns, t_{hold} = 7.0 ns, t_p = 17 ns, PRR is 50% of Enable PRR and Z_{out} ≈ 50 Ω.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 499 ± 1.0%.





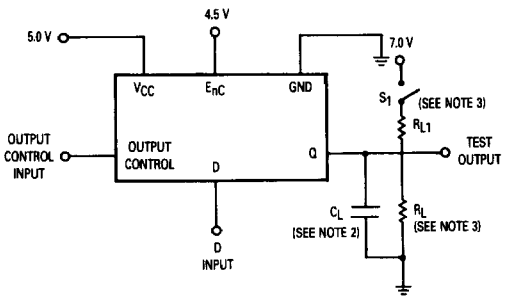
ENABLE SWITCHING TEST CIRCUIT AND WAVEFORMS





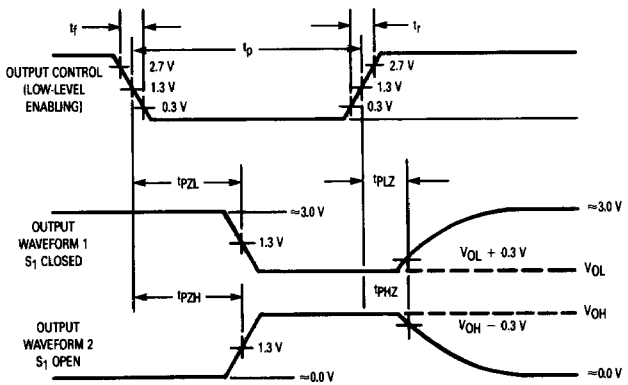
NOTES:
1. Enable input pulse characteritics: $t_r = t_f = 6.0 \pm 1.5$ ns, $t_{p(Enable)} = 10$ ns, PRR ≤ 1.0 MHz and $Z_{out} \approx 50\ \Omega$.
2. $C_L = 50$ pF ± 10% (including jig and probe capacitance).
3. $R_L = 499\ \Omega \pm 1.0\%$.

TRI-STATE SWITCHING TEST CIRCUIT AND WAVEFORMS



SWITCH POSITIONS

Symbol	S1
t_{PZH}	Open
t_{PZL}	Closed
t_{PLZ}	Closed
t_{PHZ}	Closed



NOTES:
1. Output control input pulse characteristics: $t_f = t_r = 6.0 \pm 1.5$ ns, $t_p \geq 200$ ns, PRR ≤ 1.0 ns and $Z_{out} \approx 50\ \Omega$.
2. $C_L = 50$ pF ± 10% (including jig and probe capacitance).
3. $R_L = 499\ \Omega \pm 1.0\%$.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logic "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, $\overline{OC}$ = 0.8 V, E_{nC} = 2.0 V, V_{IH} = 2.0 V, other inputs are open.
V_{OL}	Logic "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, other inputs are open, V_{IL} = 0.8 V, $\overline{OC}$ = 0.8 V, E_{nC} = 2.0 V.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open.
I_O	Output Short Circuit Current	−15	−110	−15	−110	−15	−110	mA	V_{CC} = 5.5 V, V_{IN} = 5.0 V, other inputs are open, V_{OUT} = 2.25 V, $\overline{OC}$ = GND, E_{nC} = 5.0 V.
I_{OZH}	Output Off Current High		20		20		20	μA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, other inputs are open, V_{OUT} = 2.7 V, $\overline{OC}$ = 5.0 V, E_{nC} = 5.0 V.
I_{OZL}	Output Off Current Low		−20		−20		−20	μA	V_{CC} = 5.5 V, V_{IN} = 0.8 V, other inputs are open, V_{OUT} = 0.4 V, $\overline{OC}$ = 5.0 V, E_{nC} = 5.0 V.
I_{IL}	Logical "0" Input Current	0	−100	0	−100	0	−100	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{CCH}	Power Supply Current Off		19		19		19	mA	V_{CC} = 5.5 V, V_{IN} = 5.0 V (all inputs), $\overline{OC}$ = GND.
I_{CCL}	Power Supply Current Off		24		24		24	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), E_{nC} = 5.0 V.
I_{CCZ}	Power Supply Current Off		27		27		27	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), $\overline{OC}$ = 5.0 V, E_{nC} = 5.0 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL2}	Propagation Delay /Data-Output E_{nC} to Qn	6.0	19	8.0	20	8.0	20	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output E_{nC} to Qn	8.0	20	8.0	27	8.0	27	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL3}	Propagation Delay /Data-Output Dn to Qn	2.0	12	2.0	15	2.0	15	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH3}	Propagation Delay /Data-Output Dn to Qn	2.0	12	2.0	15	2.0	15	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PZH}	Propagation Delay /Data-Output $\overline{OC}$ to Qn	4.0	18	4.0	21	4.0	21	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PZL}	Propagation Delay /Data-Output $\overline{OC}$ to Qn	4.0	18	4.0	21	4.0	21	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHZ}	Propagation Delay /Data-Output $\overline{OC}$ to Qn	2.0	8.0	2.0	10	2.0	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLZ}	Propagation Delay /Data-Output $\overline{OC}$ to Qn	3.0	13	3.0	15	3.0	15	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.