54F/74F74

Dual D-Type Positive Edge-Triggered Flip-Flop

Description

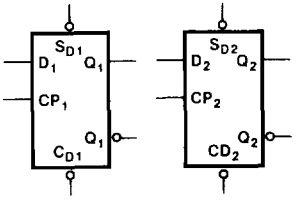
The 'F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

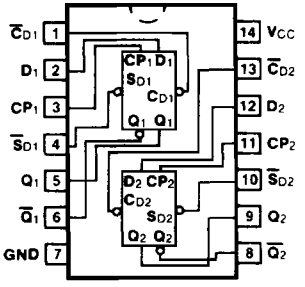
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Ordering Code: See Section 5

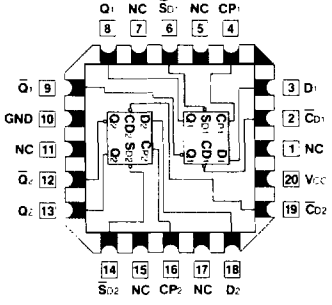
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

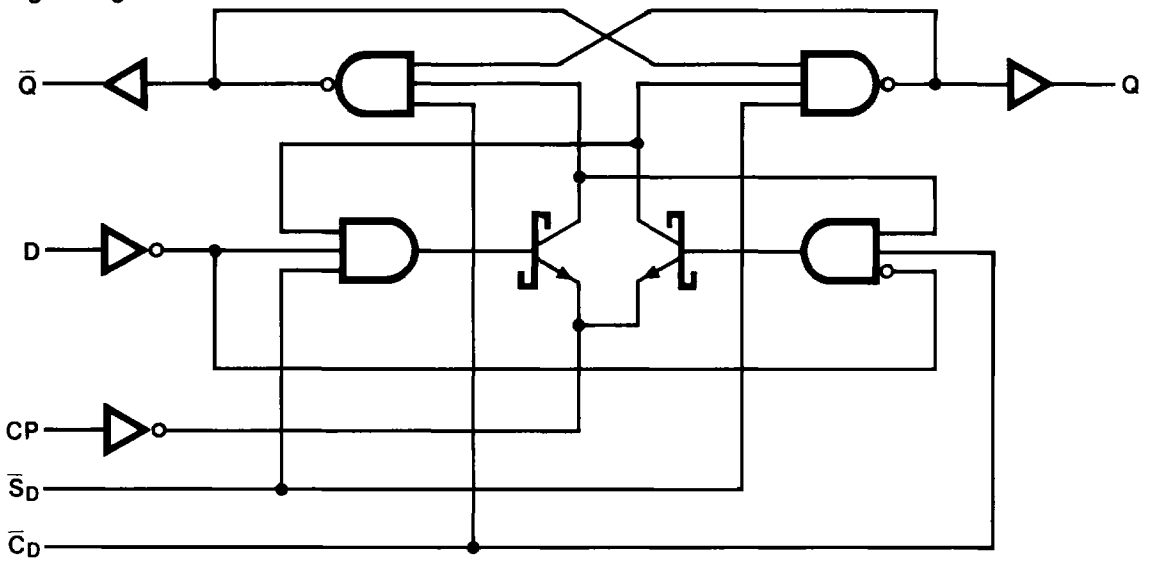
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_1, D_2	Data Inputs	0.5/0.375
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	0.5/0.375
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	0.5/1.125
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.125
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	25/12.5

Truth Table
(Each Half)

Input	Outputs	
@ t_n	@ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		10.5	16.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	125		80		100		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.8 4.4	5.3 6.2	6.8 8.0	3.8 4.4	8.5 10.5	3.8 4.4	7.8 9.2	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	8.0 11.5	3.2 3.5	7.1 10.5	ns	3-1 3-9

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP_n	2.0 3.0			3.0 4.0		2.0 3.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP_n	1.0 1.0			2.0 2.0		1.0 1.0			
$t_w(H)$ $t_w(L)$	CP_n Pulse Width HIGH or LOW	4.0 5.0			4.0 6.0		4.0 5.0		ns	3-7
$t_w(L)$	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0			4.0		4.0		ns	3-9
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0			3.0		2.0		ns	3-11