

# 54ABT/74ABT245

## Octal Bidirectional Transceiver with TRI-STATE® Outputs

### General Description

The 54ABT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA on both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a High Z condition.

### Features

- Bidirectional non-inverting buffers
- A and B output sink capability of 64 mA, source capability of 32 mA

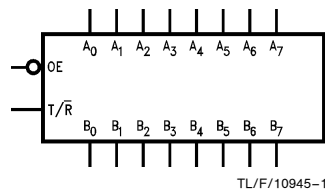
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time is less than enable time to avoid bus contention
- Standard Military Drawing (SMD) 5962-9214801

Commercial	Military	Package Number	Package Description
74ABT245CSC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74ABT245CSJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
74ABT245CPC		N20B	20-Lead (0.300" Wide) Molded Dual-In-Line
	54ABT245J/883	J20A	20-Lead Ceramic Dual-In-Line
74ABT245CMSA (Note 1)		MSA20	20-Lead Molded Shrink Small Outline, EIAJ Type II
	54ABT245W/883	W20A	20-Lead Cerpak
	54ABT245E/883	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74ABT245CMT (Notes 1, 2)		MTC20	20-Lead Molded Thin Shrink Small Outline, JEDEC

**Note 1:** Devices also available in 13" reel. Use suffix = SCX, SJX, MSAX, and MTCX.

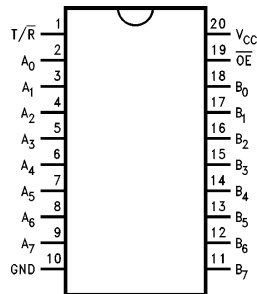
**Note 2:** Contact factory for package availability.

### Logic Symbol

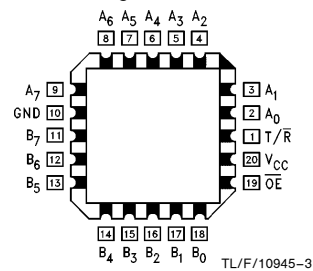


### Connection Diagrams

Pin Assignment for DIP, Flatpak, SSOP and SOIC



Pin Assignment for LCC



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## Pin Descriptions

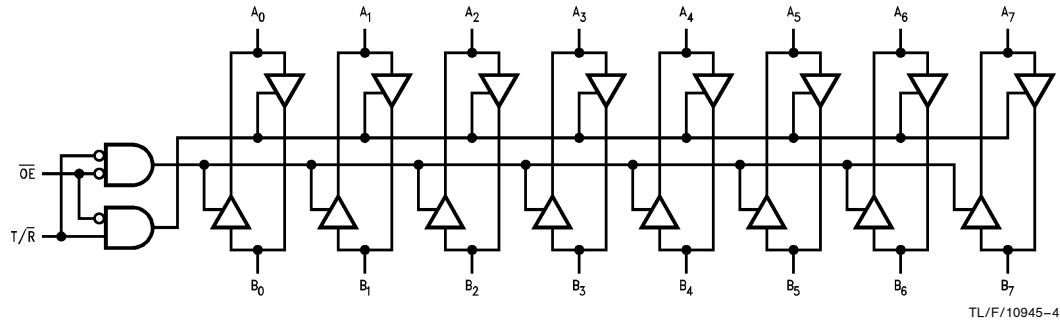
Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/ $\overline{R}$	Transmit/Receive Input
A <sub>0</sub> -A <sub>7</sub>	Side A Inputs or TRI-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Side B Inputs or TRI-STATE Outputs

## Truth Table

Inputs		Output
$\overline{OE}$	T/ $\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

## Logic Diagram



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State in the HIGH State	-0.5V to 5.5V -0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	-40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	( $\Delta V/\Delta t$ )
Data Input	50 mV/ns
Enable Input	20 mV/ns

## DC Electrical Characteristics

Symbol	Parameter		ABT245			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage		0.8			V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage		-1.2			V	Min	I <sub>IN</sub> = -18 mA ( $\overline{OE}$ , T/ $\overline{R}$ )
V <sub>OH</sub>	Output HIGH Voltage	54ABT/74ABT	2.5		V	Min	I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> )	
		54ABT	2.0		V	Min	I <sub>OH</sub> = -24 mA (A <sub>n</sub> , B <sub>n</sub> )	
		74ABT	2.0		V	Min	I <sub>OH</sub> = -32 mA (A <sub>n</sub> , B <sub>n</sub> )	
V <sub>OL</sub>	Output LOW Voltage	54ABT	0.55		V	Min	I <sub>OL</sub> = 48 mA (A <sub>n</sub> , B <sub>n</sub> )	
		74ABT	0.55				I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )	
I <sub>IH</sub>	Input HIGH Current		5		μA	Max	V <sub>IN</sub> = 2.7V ( $\overline{OE}$ , T/ $\overline{R}$ ) (Note 3) V <sub>IN</sub> = V <sub>CC</sub> ( $\overline{OE}$ , T/ $\overline{R}$ )	
		5						
I <sub>BVI</sub>	Input HIGH Current Breakdown Test		7		μA	Max	V <sub>IN</sub> = 7.0V ( $\overline{OE}$ , T/ $\overline{R}$ )	
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)		100		μA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )	
I <sub>IL</sub>	Input LOW Current		-5		μA	Max	V <sub>IN</sub> = 0.5V ( $\overline{OE}$ , T/ $\overline{R}$ ) (Note 3) V <sub>IN</sub> = 0.0V ( $\overline{OE}$ , T/ $\overline{R}$ )	
		-5						
V <sub>ID</sub>	Input Leakage Test		4.75		V	0.0	I <sub>ID</sub> = 1.9 μA ( $\overline{OE}$ , T/ $\overline{R}$ ) All Other Pins Grounded	
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current		50		μA	0 - 5.5V	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> ); $\overline{OE}$ = 2.0V	
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current		-50		μA	0 - 5.5V	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> ); $\overline{OE}$ = 2.0V	
I <sub>OS</sub>	Output Short-Circuit Current		-100		mA	Max	V <sub>OUT</sub> = 0.0V (A <sub>n</sub> , B <sub>n</sub> )	
I <sub>CEX</sub>	Output High Leakage Current		50		μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )	
I <sub>ZZ</sub>	Bus Drainage Test		100		μA	0.0	V <sub>OUT</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> ); All Others GND	
I <sub>CCH</sub>	Power Supply Current		50		μA	Max	All Outputs HIGH	
I <sub>CCL</sub>	Power Supply Current		30		mA	Max	All Outputs LOW	
I <sub>CCZ</sub>	Power Supply Current		50		μA	Max	$\overline{OE}$ = V <sub>CC</sub> , T/ $\overline{R}$ = GND or V <sub>CC</sub> ; All Other GND or V <sub>CC</sub>	

**Note 3:** Guaranteed but not tested.

## DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT245			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>CC</sub> T	Additional Outputs Enabled I <sub>CC</sub> /Input Outputs TRI-STATE Outputs TRI-STATE			2.5 2.5 50	mA mA μA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V OE, T/ $\bar{R}$ V <sub>I</sub> = V <sub>CC</sub> - 2.1V Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Others at V <sub>CC</sub> or GND.
I <sub>CC</sub> D	Dynamic I <sub>CC</sub> No Load (Note 2)			0.1	mA/ MHz	Max	Outputs Open OE = GND, T/ $\bar{R}$ = GND or V <sub>CC</sub> One Bit Toggling, 50% Duty Cycle (Note 1)

**Note 1:** For 8 bits toggling, I<sub>CC</sub>D < 0.8 mA/MHz.

**Note 2:** Guaranteed, but not tested.

## DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
							C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>		0.7	1.0	V	5.0	T <sub>A</sub> = 25°C (Note 1)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-1.3	-1.0		V	5.0	T <sub>A</sub> = 25°C (Note 1)
V <sub>OHV</sub>	Minimum High Level Dynamic Output Voltage	2.7	3.1		V	5.0	T <sub>A</sub> = 25°C (Note 3)
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	T <sub>A</sub> = 25°C (Note 2)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		0.9	0.6	V	5.0	T <sub>A</sub> = 25°C (Note 2)

**Note 1:** Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

**Note 2:** Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). Guaranteed, but not tested.

**Note 3:** Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

## AC Electrical Characteristics (SOIC and SSOP package)

Symbol	Parameter	74ABT			54ABT		74ABT		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	1.0	2.1	3.6	1.0	4.8	1.0	3.6	ns
t <sub>PHL</sub>	Data to Outputs	1.0	2.4	3.6	1.0	4.8	1.0	3.6	
t <sub>PZH</sub>	Output Enable	1.5	3.2	6.0	1.0	6.7	1.5	6.0	ns
t <sub>PZL</sub>	Time	1.5	3.7	6.0	2.0	7.5	1.5	6.0	
t <sub>PHZ</sub>	Output Disable	1.0	3.6	6.1	1.7	7.4	1.0	6.1	ns
t <sub>PLZ</sub>	Time	1.0	3.3	5.6	1.7	6.5	1.0	5.6	

## Extended AC Electrical Characteristics (SOIC package)

Symbol	Parameter	74ABT			74ABT		74ABT		Units
		-40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF 8 Outputs Switching (Note 4)			T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 250 pF 1 Output Switching (Note 5)		T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 250 pF 8 Outputs Switching (Note 6)		
		Min	Typ	Max	Min	Max	Min	Max	
f <sub>toggle</sub>	Max Toggle Frequency		100						MHz
t <sub>PLH</sub>	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.5	ns
t <sub>PHL</sub>	Data to Outputs	1.5		5.0	1.5	6.0	2.5	8.5	

## Extended AC Electrical Characteristics (SOIC package)

Symbol	Parameter	74ABT			74ABT		74ABT		Units
		-40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF 8 Outputs Switching (Note 4)			T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 250 pF 1 Output Switching (Note 5)		T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 250 pF 8 Outputs Switching (Note 6)		
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PZH</sub>	Output Enable Time	1.5		6.5	2.5	7.5	2.5	9.5	ns
t <sub>PZL</sub>		1.5		6.5	2.5	7.5	2.5	11.0	
t <sub>PHZ</sub>	Output Disable Time	1.0		6.5	(Note 7)		(Note 7)		ns
t <sub>PLZ</sub>		1.0		5.6					

**Note 4:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

**Note 5:** This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

**Note 6:** This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

**Note 7:** The TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

## Skew (SOIC package)

Symbol	Parameter	74ABT		Units		
		T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF 8 Outputs Switching (Note 3)			T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 250 pF 8 Outputs Switching (Note 4)	
		Max			Max	
t <sub>OSSL</sub> (Note 1)	Pin to Pin Skew HL Transitions	1.3		2.3	ns	
t <sub>OSLH</sub> (Note 1)	Pin to Pin Skew LH Transitions	1.0		1.8	ns	
t <sub>PS</sub> (Note 5)	Duty Cycle LH-HL Skew	2.0		3.5	ns	
t <sub>OST</sub> (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0		3.5	ns	
t <sub>PV</sub> (Note 2)	Device to Device Skew LH/HL Transitions	2.0		3.5	ns	

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t<sub>OSSL</sub>), LOW to HIGH (t<sub>OSLH</sub>), or any combination switching LOW to HIGH and/or HIGH to LOW (t<sub>OST</sub>). The specification is guaranteed but not tested.

**Note 2:** Propagation delay variation for a given set of conditions (i.e., temperature and V<sub>CC</sub>) from device to device. This specification is guaranteed but not tested.

**Note 3:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

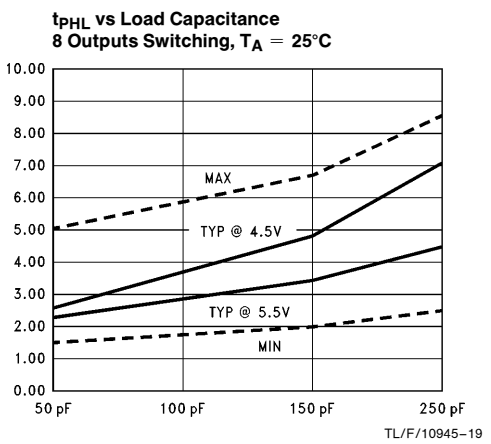
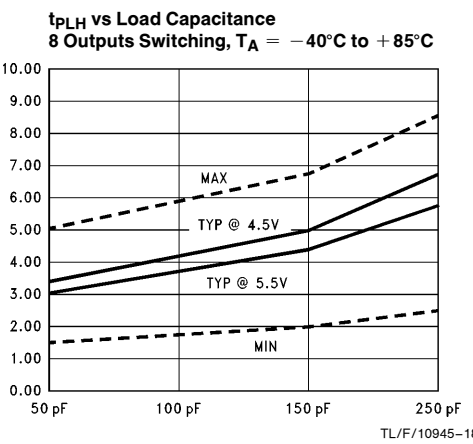
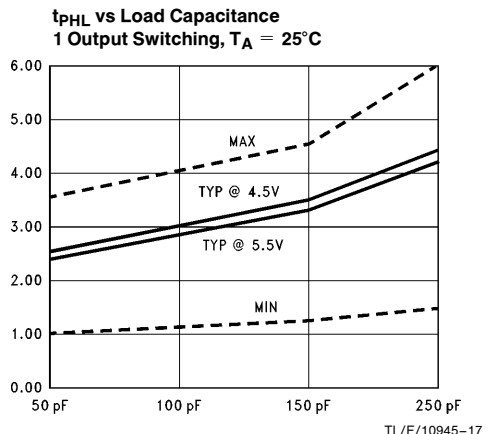
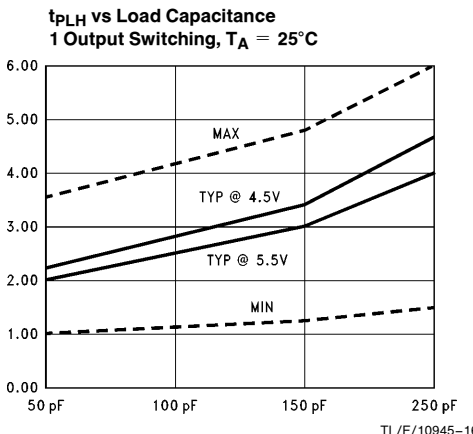
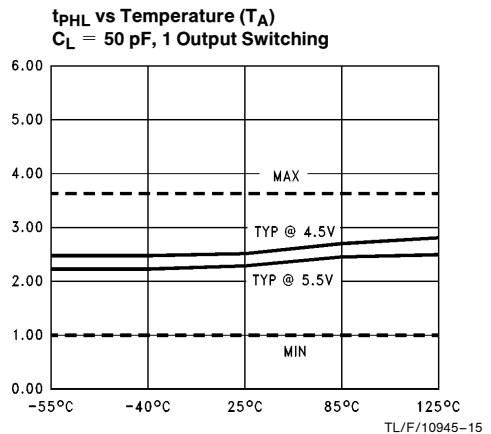
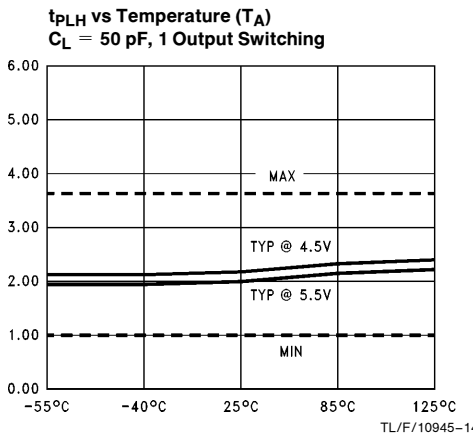
**Note 4:** These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

**Note 5:** This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

## Capacitance

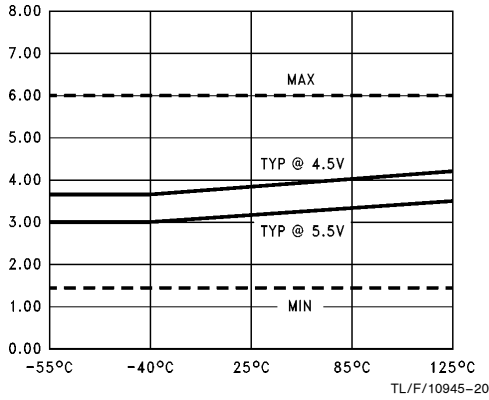
Symbol	Parameter	Typ	Units	Conditions T <sub>A</sub> = 25°C
C <sub>IN</sub>	Input Capacitance	5.0	pF	V <sub>CC</sub> = 0V ( $\overline{OE}$ , T/ $\overline{R}$ )
C <sub>I/O</sub> (Note 1)	I/O Capacitance	11.0	pF	V <sub>CC</sub> = 5.0V (A <sub>n</sub> , B <sub>n</sub> )

**Note 1:** C<sub>I/O</sub> is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

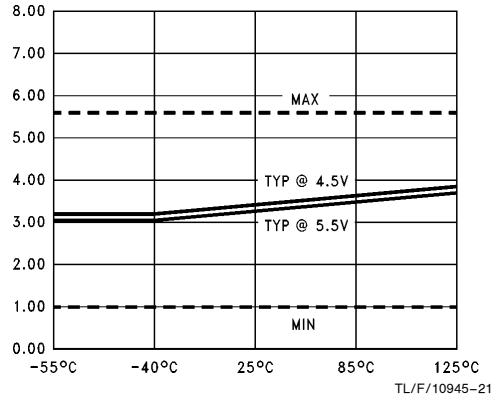


Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

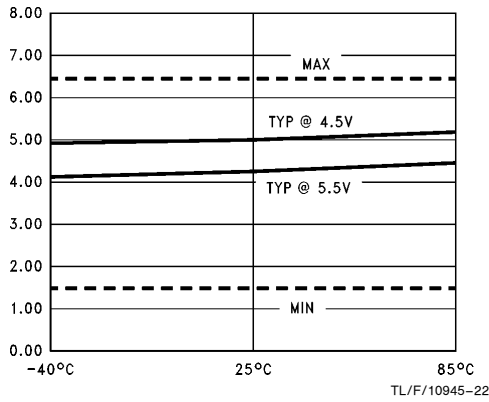
**$t_{pZL}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching



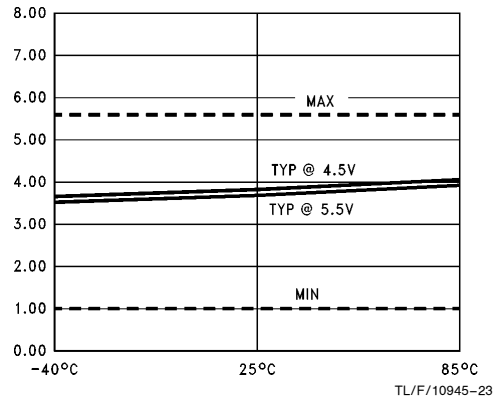
**$t_{pLZ}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching



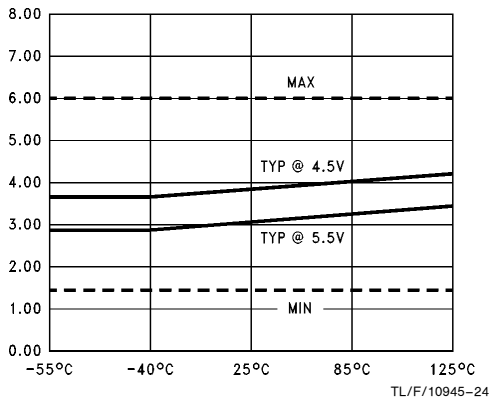
**$t_{pZL}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 8 Outputs Switching



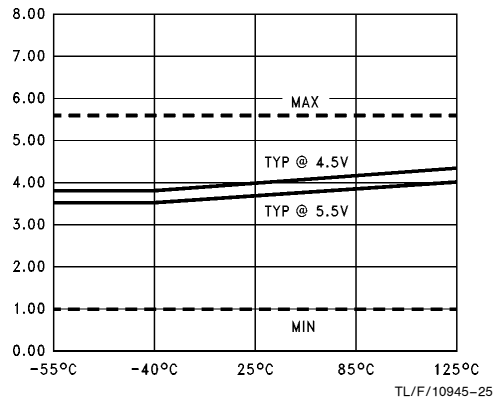
**$t_{pLZ}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 8 Outputs Switching



**$t_{pZH}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching

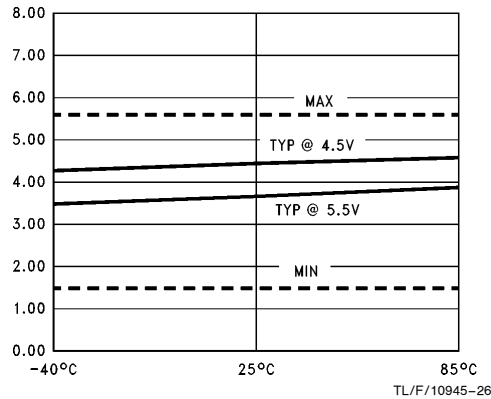


**$t_{pHZ}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching

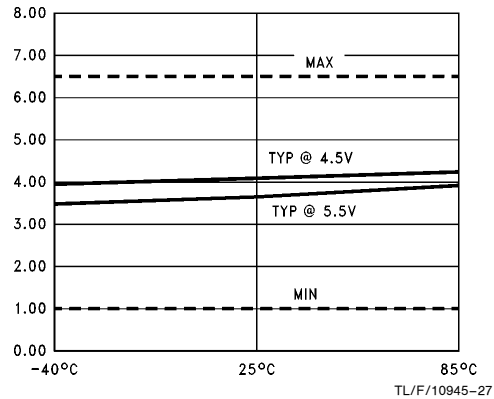


Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

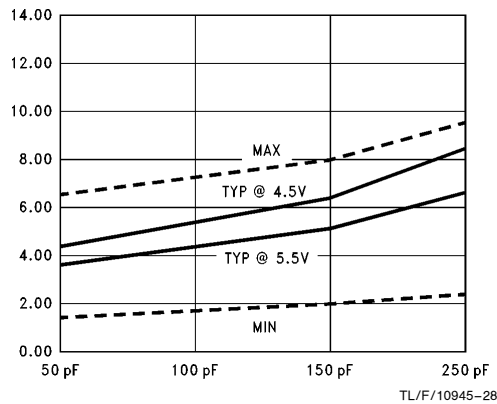
**tpZH vs Temperature (TA)**  
 CL = 50 pF, 8 Outputs Switching



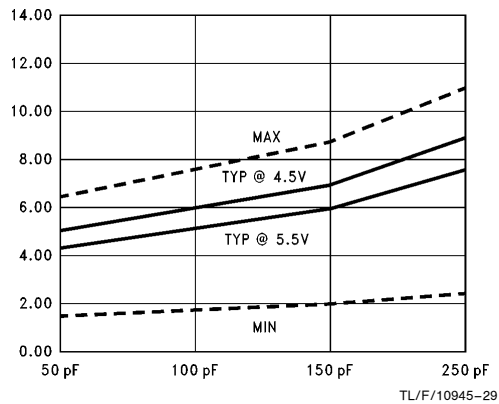
**tpHZ vs Temperature (TA)**  
 CL = 50 pF, 8 Outputs Switching



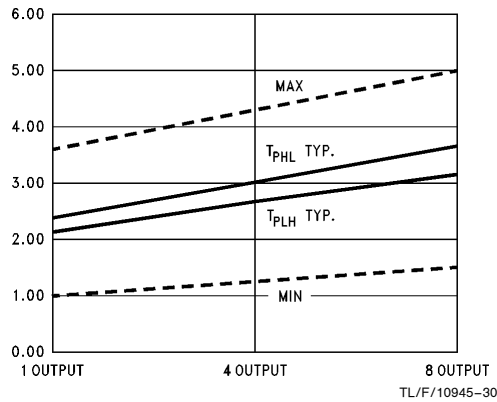
**tpZH vs Load Capacitance**  
 8 Outputs Switching, TA = 25°C



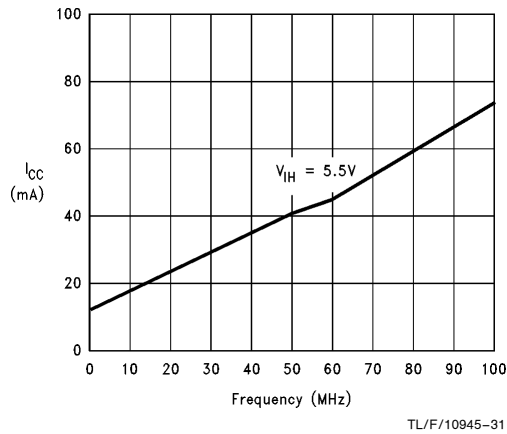
**tpZL vs Load Capacitance**  
 8 Outputs Switching, TA = 25°C



**tpLH and tpHL vs Number Outputs Switching**  
 VCC = 5.0V, TA = 25°C, CL = 50 pF



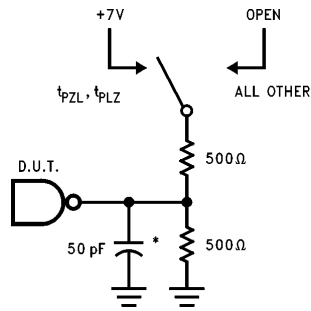
**ICC vs Frequency, Average, TA = 25°C,**  
 All Outputs Unloaded/Unterminated



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.



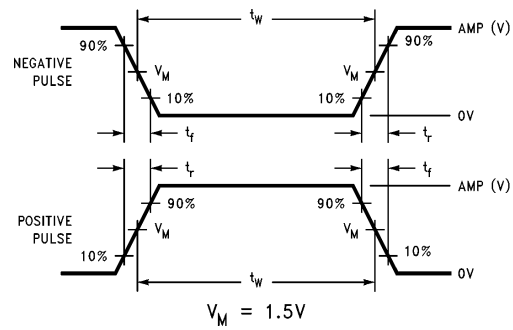
## AC Loading



TL/F/10945-6

\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load



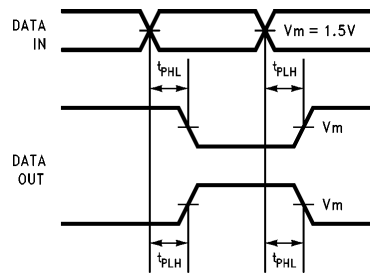
TL/F/10945-7

FIGURE 2a. Test Input Signal Levels

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

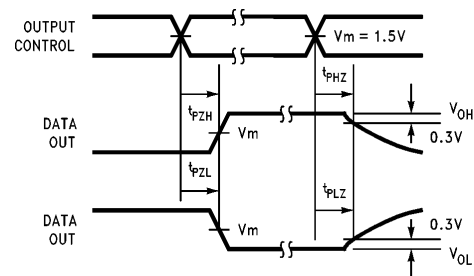
FIGURE 2b. Test Input Signal Requirements

## AC Waveforms



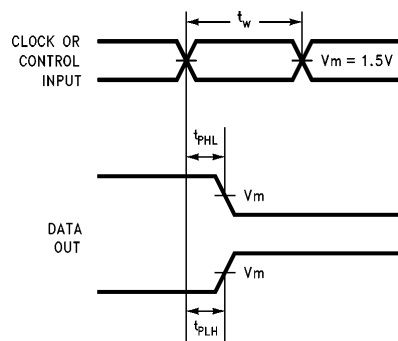
TL/F/10945-8

FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions



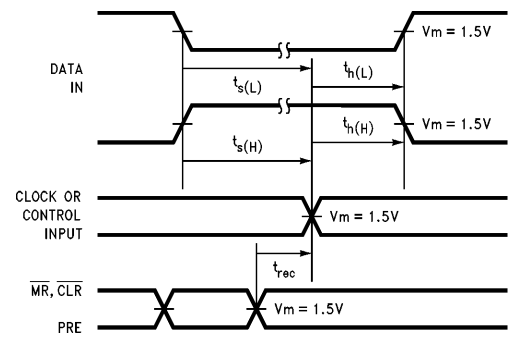
TL/F/10945-10

FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times



TL/F/10945-9

FIGURE 4. Propagation Delay, Pulse Width Waveforms

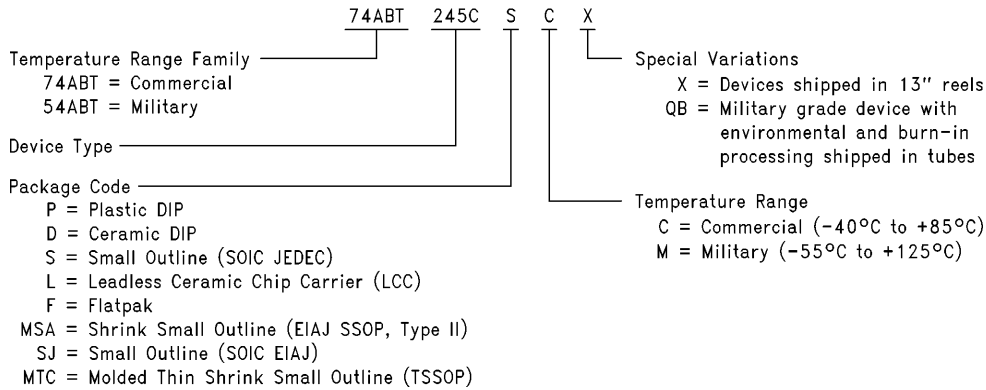


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FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

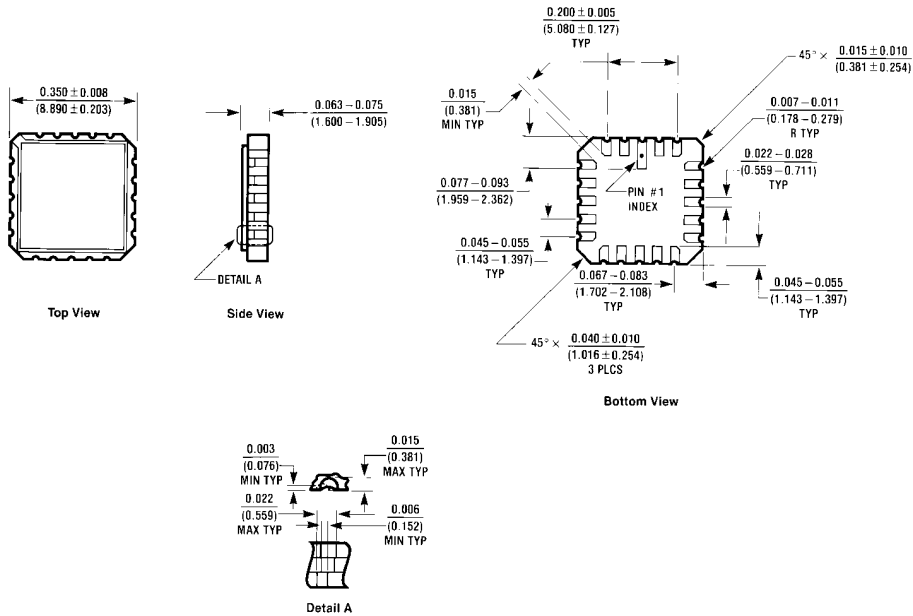
## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/10945-32

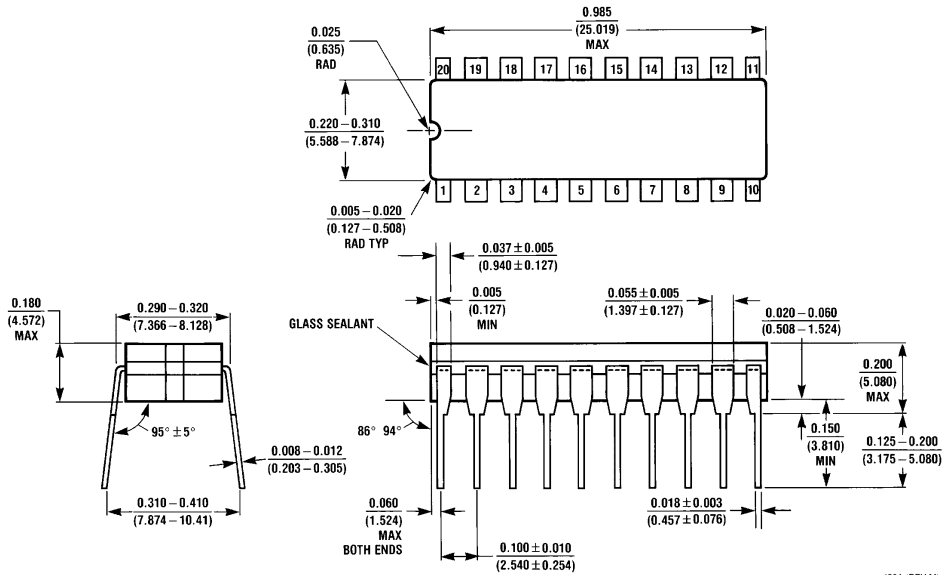
## Physical Dimensions inches (millimeters)



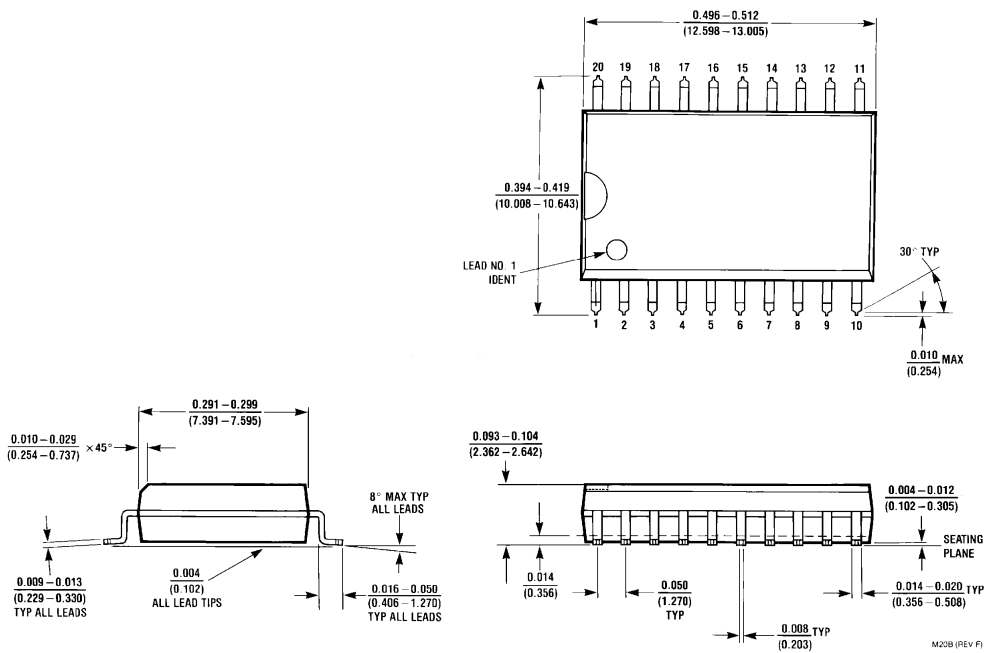
20-Terminal Ceramic Chip Carrier (L)  
NS Package Number E20A

L704-REV. 01

**Physical Dimensions** inches (millimeters) (Continued)

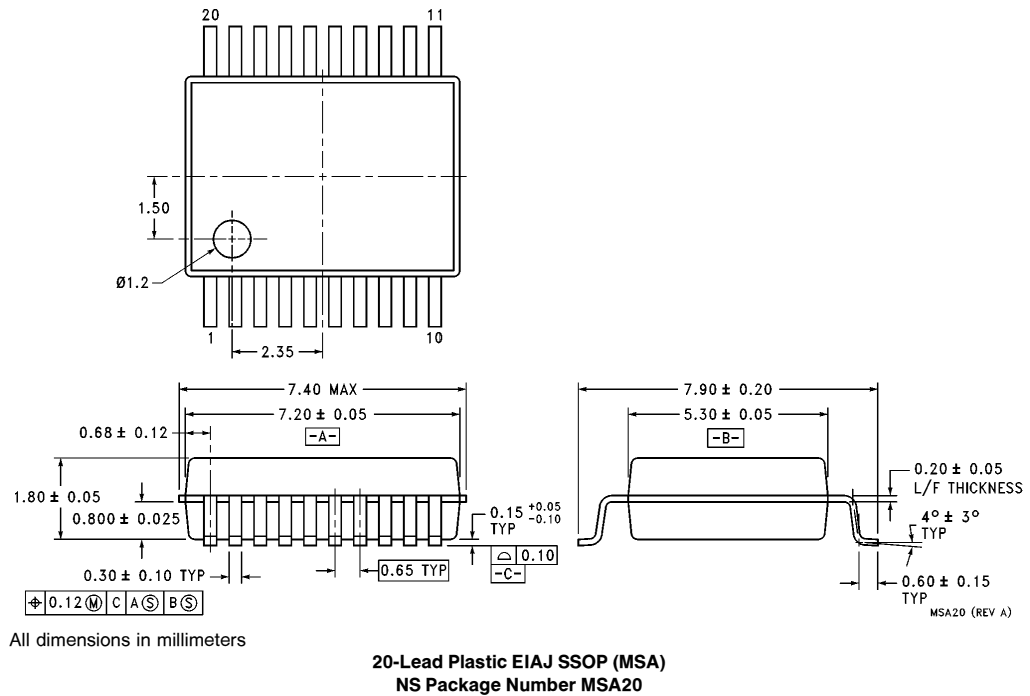
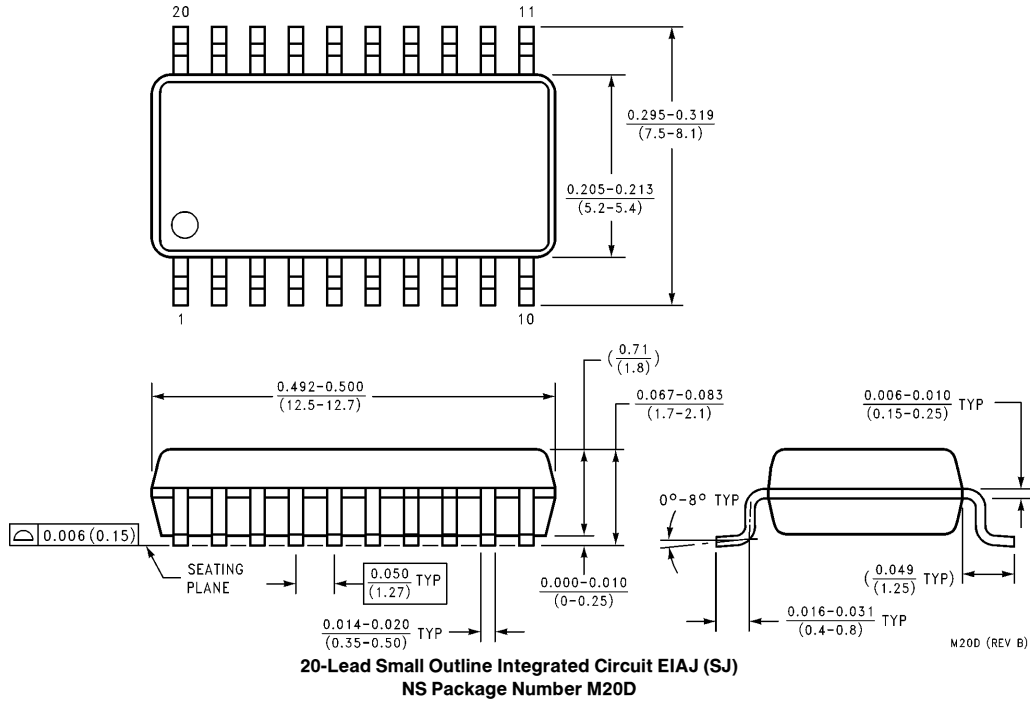


**20-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J20A

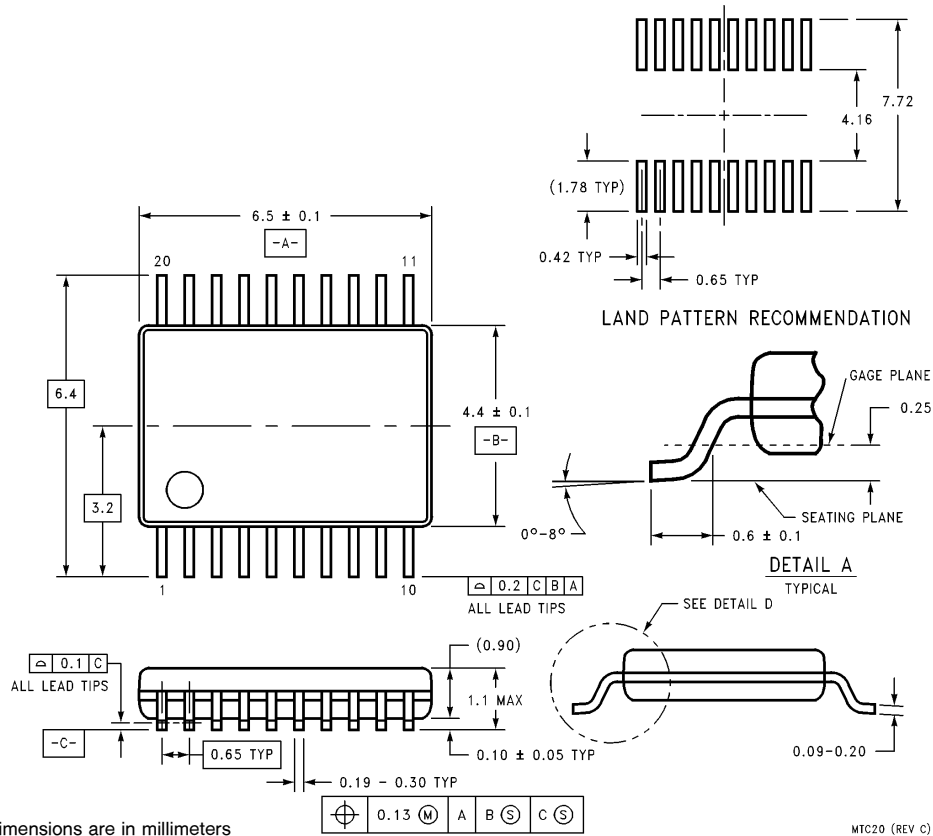


**20-Lead Small Outline Integrated Circuit JEDEC (S)**  
NS Package Number M20B

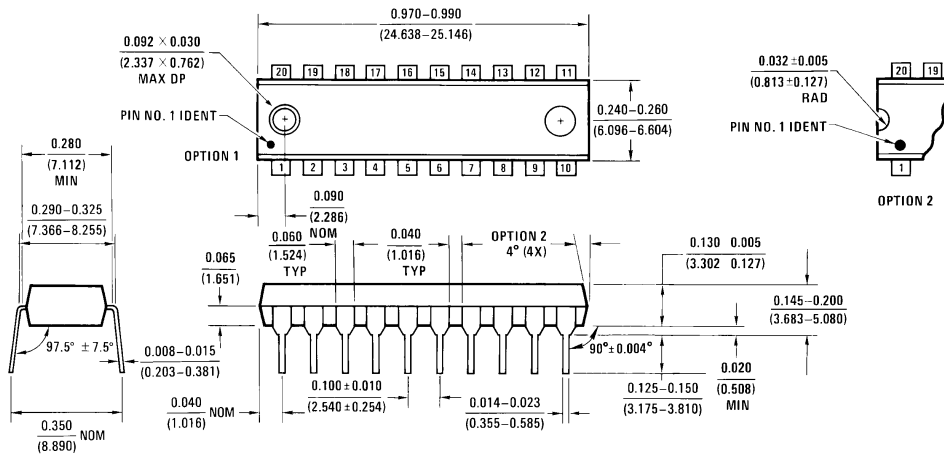
**Physical Dimensions** inches (millimeters) (Continued)



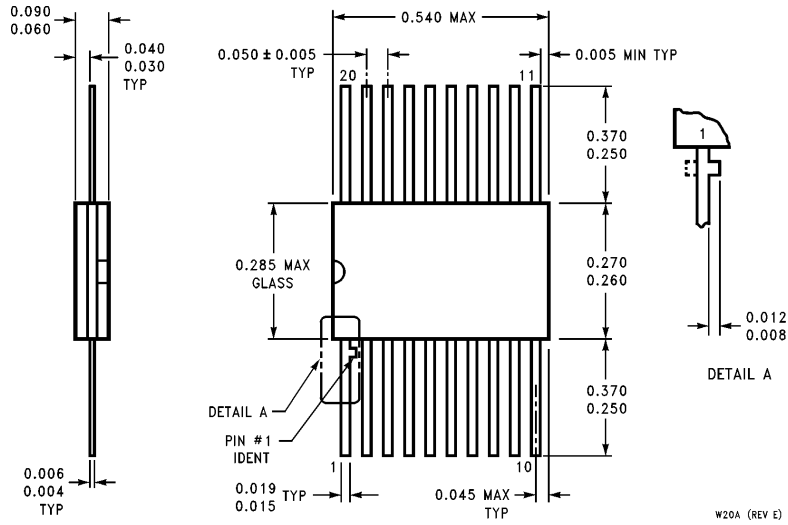
**Physical Dimensions** inches (millimeters) (Continued)



**20-Lead Molded Thin Shrink Small Outline Package, JEDEC  
NS Package Number MTC20**



**Physical Dimensions** inches (millimeters) (Continued)



**20-Lead Ceramic Flatpak (F)  
NS Package Number W20A**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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