Octal dual supply translating transceiver; 3-state — 74LVC4245

FEATURES

- **Wide supply voltage range**
  3 Volt port: 1.5 to 3.6 V
  5 Volt port: 1.5 to 5.5 V
- **In accordance with JEDEC standard no. 8-1A.**
- **Control inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74LVC4245 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC4245 is an octal dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.
It is designed to interface between a 3 V bus and 5 V bus in a mixed 3 V/5 V supply environment.

The '4245' features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectivly isolated.

In suspend mode, when V_{CCA} is zero, there will be no current flow from one supply to the other supply. The A-outputs must be set 3-state and the voltage on the A bus must be smaller then V_{diode} (typ. 0.7V). $V_{CCA} \geq V_{CCB}$ (except in suspend mode).

FUNCTION TABLE

INPUTS		OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nB nB to nA	C_L = 50 pF V_{CCA} = 5.0 V V_{CCB} = 3.3 V	 4.0 4.0	ns
$C_{I/O}$	input/output capacitance		10	pF
C_{PDA}	A port nA to nB A port nB to nA	notes 1 and 2	7.8 27.9	pF
C_{PDB}	B port nA to nB B port nB to nA		26 10.4	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC4245D	24	SO	plastic	SOT137-1
74LVC4245DB	24	SSOP	plastic	SOT340-1
74LVC4245PW	24	TSSOP	plastic	SOT355-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{CCA}	positive supply voltage (5 V bus)
2	DIR	direction control
3, 4, 5, 6, 7, 8, 9, 10	A_0 to A_7	data inputs/outputs
11, 12, 13	GND	GND
14, 15, 16, 17, 18, 19, 20, 21	B_7 to B_0	data inputs/outputs
22	$\overline{OE}$	output enable input (active LOW)
23, 24	V_{CCB}	positive supply voltage (3 V bus)

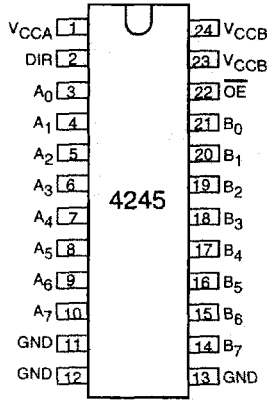


Fig.1 Pin configuration.

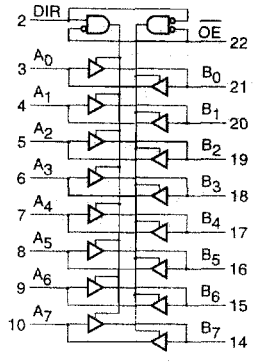


Fig.2 Logic symbol.

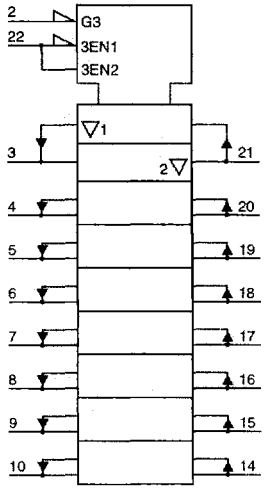


Fig.3 IEC Logic symbol.

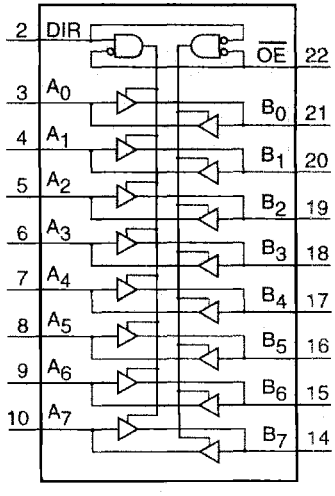


Fig.4 Functional diagram.

RECOMMENDED OPERATING CONDITIONS FOR THE 74LVC4245

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CCA}	DC supply voltage 5 V port	1.5	5.5	V	see Fig.8 $V_{CCA} \geq V_{CCB}$
V_{CCB}	DC supply voltage 3 V port	1.5	3.6	V	see Fig.8 $V_{CCA} \geq V_{CCB}$
V_I	DC input voltage range (control inputs)	0	5.5	V	
$V_{I/O}$	DC input voltage range for I/Os	0	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	−40	+85	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times	0 0 0 0	20 10 20 10	ns/V	V_{CCB} = 2.7 to 3.0 V V_{CCB} = 3.0 to 3.6 V V_{CCA} 3.0 to 4.5 V V_{CCA} 4.5 to 5.5 V

LIMITING VALUES FOR THE 74LVC4245 (Note 1)

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CCA}	DC supply voltage 5 V port	−0.5	+6.5	V	
V_{CCB}	DC supply voltage 3 V port	−0.5	+4.6	V	
I_{IK}	DC input diode current	–	−50	mA	$V_I < 0$
V_I	DC input voltage	−0.5	+5.5	V	note 2
$V_{I/O}$	DC input voltage range for I/Os	−0.5	V_{CC} + 0.5	V	
I_{OK}	DC output diode current	–	±50	mA	$V_O > V_{CC}$ or $V_O < 0$
V_O	DC output voltage	−0.5	V_{CC} + 0.5	V	note 2
I_O	DC output source or sink current	–	±50	mA	V_O = 0 to V_{CC}
I_{GND}, I_{CC}	DC V_{CC} or GND current	–	±100	mA	
T_{stg}	storage temperature range	−60	+150	°C	
P_{tot}	power dissipation per package - plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	– –	500 500	mW	above + 70°C derate linearly with 8 mW/K above + 60°C derate linearly with 5.5 mW/K

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE 74LVC4245

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS		
		MIN.	TYP.	MAX.		$V_{CCA/B}$ (V)	V_I	OTHER
V_{IH}	HIGH level input voltage (3 V port)	2.0	–	–	V	2.7 to 3.6		
V_{IH}	HIGH level input voltage (5 V port)	2.0	–	–	V	4.5 to 5.5		
V_{IL}	LOW level input voltage (3 V port)	–	–	0.8	V	2.7 to 3.6		
V_{IL}	LOW level input voltage (5 V port)	–	–	0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage (3 V port)	V_{CC} − 0.2 V_{CC} − 1.0 V_{CC} − 0.5	V_{CC} – –	– – –	V	3.0 3.0 2.7	V_{IH} or V_{IL}	I_O = −100 mA I_O = −24 µA I_O = −12 mA
V_{OH}	HIGH level output voltage (5 V port)	V_{CC} − 0.2 V_{CC} − 0.8 V_{CC} − 0.5	V_{CC} – –	– – –	V	4.5 4.5 4.5	V_{IH} or V_{IL}	I_O = −100 µA I_O = −24 mA I_O = −12 mA
V_{OL}	LOW level output voltage (3 V port)	– – –	– – –	0.20 0.55 0.40	V	3.0 3.0 2.7	V_{IH} or V_{IL}	I_O = 100 mA I_O = 24 µA I_O = 12 mA
V_{OL}	LOW level output voltage (5 V port)	– – –	– – –	0.20 0.55 0.40	V	4.5 4.5 4.5	V_{IH} or V_{IL}	I_O = 100 mA I_O = 24 µA I_O = 12 mA
I_I	input leakage current (control inputs)	–	±0.1	±5	µA	3.6	5.5 V or GND	not for I/O pins
I_{IHZ}/I_{ILZ}	input current for common I/O pins (3 V port)	–	±0.1	±15	µA	3.6	V_{CC} or GND	
I_{IHZ}/I_{ILZ}	input current for common I/O pins (5 V port)	–	±0.1	±15	µA	5.5	V_{CC} or GND	
I_{OZ}	3-state output OFF-state current (3 V port)	–	0.1	±10	µA	3.6	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{OZ}	3-state output OFF-state current (5 V port)	–	0.1	±10	µA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current (3 V port)	–	0.1	20	µA	3.6	V_{CC} or GND	I_O = 0
I_{CC}	quiescent supply current (5 V port)	–	0.1	20	µA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current given per input pin (3 V port)	–	5	500	µA	2.7 to 3.6	V_{CC} − 0.6 V	I_O = 0
ΔI_{CC}	additional quiescent supply current given per input pin (5 V port)	–	5	500	µA	4.5 to 5.5	V_{CC} − 2.1 V	I_O = 0

Note: All typical values are measured at V_{CCA} = 5.0 V, V_{CCB} = 3.3 V and T_{amb} = 25 °C.

DC CHARACTERISTICS FOR 74LVC4245

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC4245

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS		
		MIN.	TYP.	MAX.		V_{CCA} (V)	V_{CCB} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n to B_n	1.5 1.5	4.5 4.0*	7.0 6.5	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Figs 5, 7
t_{PHL}/t_{PLH}	propagation delay B_n to A_n	1.5 1.5	4.5 4.0*	7.0 6.5	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Figs 5, 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n	1.5 1.5	7.0 6.2*	11 10	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Figs 6, 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to B_n	1.5 1.5	5.7 5.0*	8.7 8.1	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Figs 6, 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n	1.5 1.5	5.7 5.3*	8.0 7.5	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Figs 6, 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to B_n	1.5 1.5	6.2 5.8*	8.5 7.8	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Figs 6, 7

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CCA} = 5.0$ V and $V_{CCB} = 3.3$ V.

AC WAVEFORMS

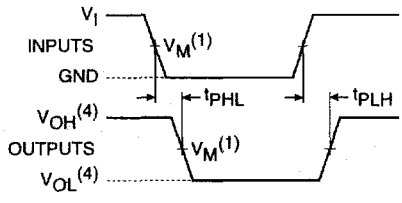


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

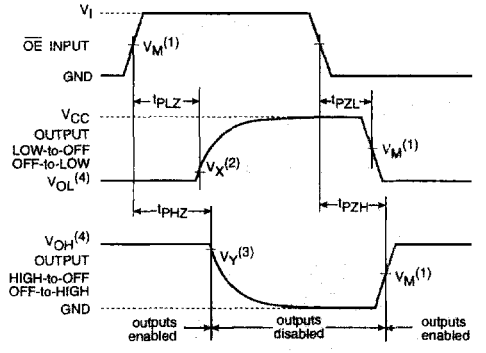
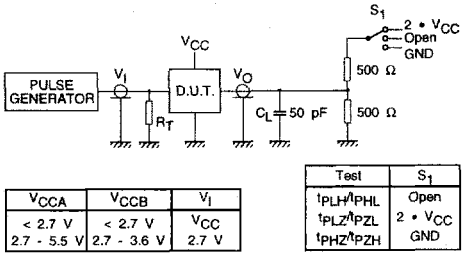


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CCA}	V_{CCB}	V_I
< 2.7 V	< 2.7 V	V_{CC}
2.7 - 5.5 V	2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

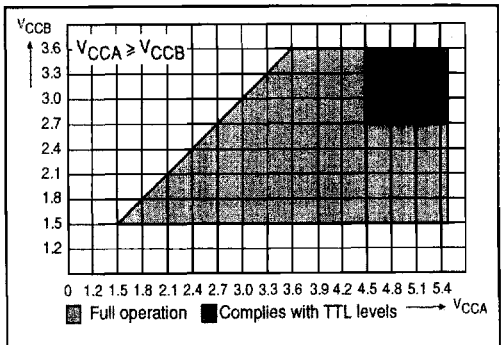


Fig.8 Supply operating area.

Notes:

(1) V_M = 1.5 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_M = 0.5 . V_{CCA} at V_{CCA} ≥ 4.5 V

(2) V_X = V_{OL} + 0.3 V at V_{CC} ≤ 3.6 V
V_X = V_{OL} + 0.1 · (V_{CC} – V_{OL}) at V_{CCA} ≥ 4.5 V

(3) V_Y = V_{OH} – 0.3 V at V_{CC} ≤ 3.6 V
V_Y = V_{OH} – 0.1 · (V_{OH} – GND) at V_{CCA} ≥ 4.5 V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.