

**KS54HCTLS 42**  
**KS74HCTLS**

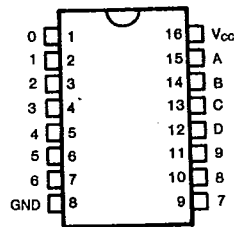
**BCD-to Decimal Decoder**

T-67-21-57

**FEATURES**

- Full decoding of Input Logic
- All outputs are High for Invalid BCD Conditions
- Also for application as 3-Line to 8-Line Decoders
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

**PIN CONFIGURATION**



**FUNCTION TABLE**

No.	Inputs				Outputs										
	D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H
3	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H
5	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H
6	L	H	H	L	H	H	H	H	H	L	H	H	H	H	H
7	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H
8	H	L	L	L	H	H	H	H	H	H	H	L	H	H	H
9	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

**DESCRIPTION**

The '42 decoder accepts for active-high BCD inputs and provides 10 mutually exclusive active-low outputs, as shown by logic symbol or diagram. The active-low outputs facilitate addressing other MSI units with active-low input enables.

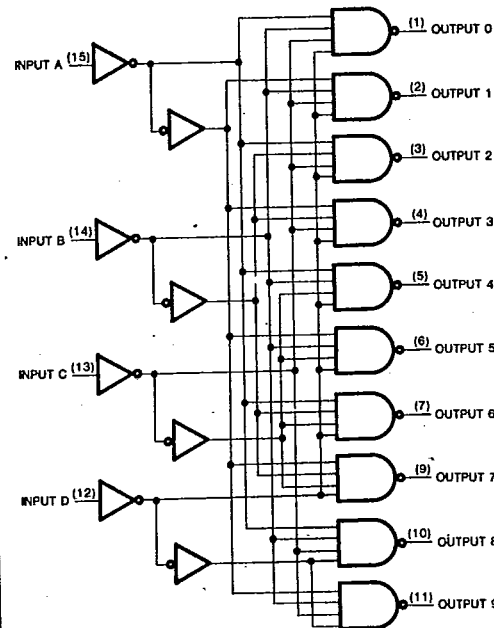
The logic design of the '42 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant input, D, produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The D input can also be used as the Data Input in an 8-output demultiplexer application.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



**KS54HCTLS 42**  
**KS74HCTLS**

**BCD-to Decimal Decoder**

T-67-21-57

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C  
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns), HCTLS42

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay Any Input to Y	$t_{PLH}$	$C_L = 50\text{pF}$	19	25	32	38	ns
	$t_{PHL}$		19	25	32	38	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)					pF

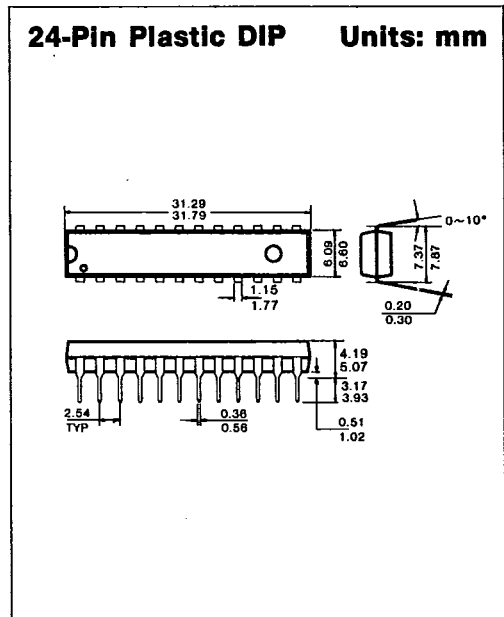
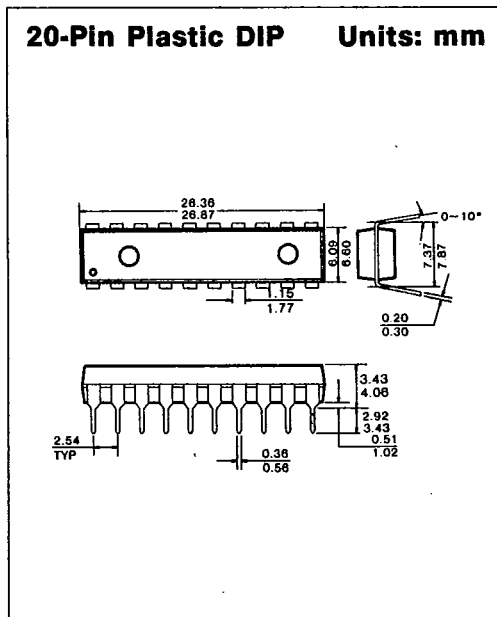
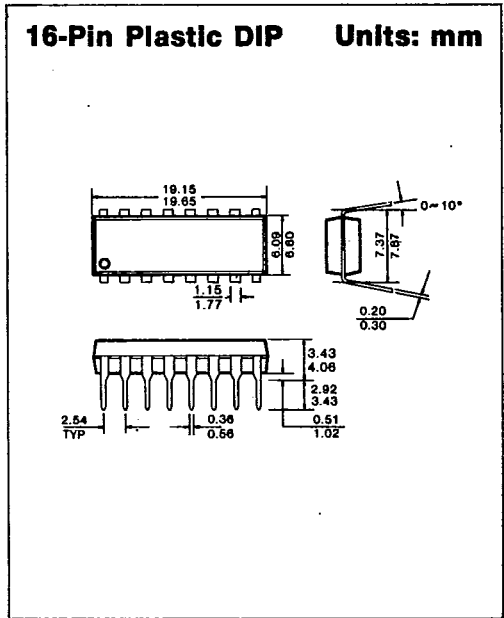
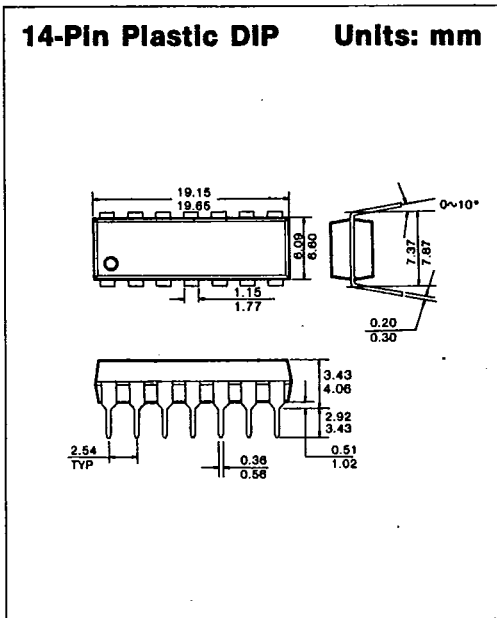
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

† For AC switching test circuits and timing waveforms see section 2.

**PACKAGE DIMENSIONS**

T-90-20

**1. PLASTIC PACKAGES**

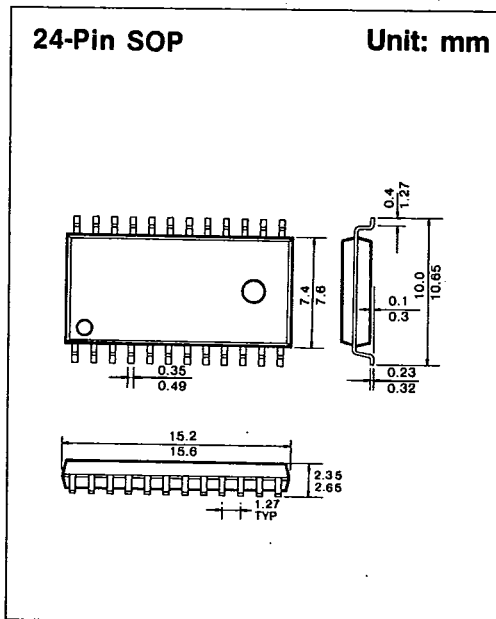
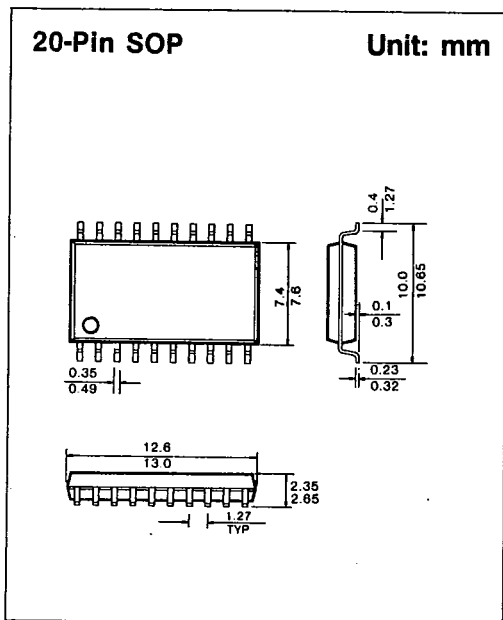
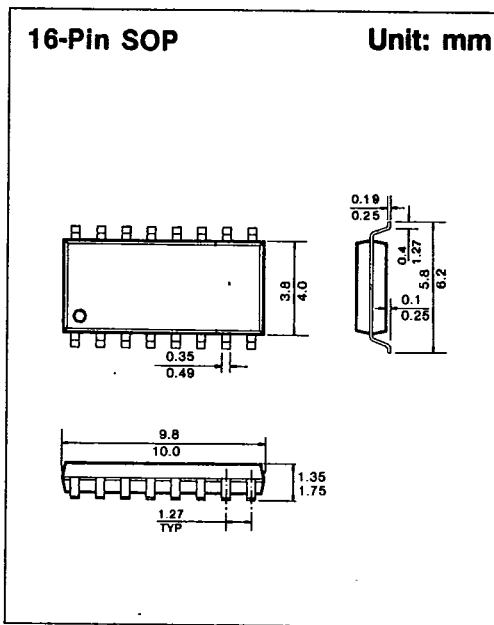
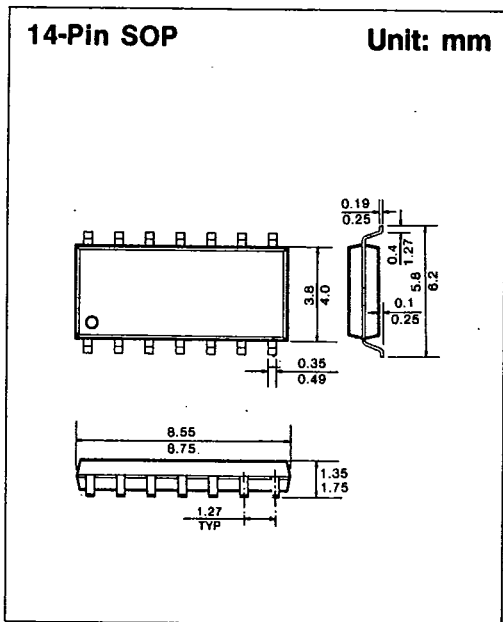


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**PACKAGE DIMENSIONS**

T-90-20



**PACKAGE DIMENSIONS**

T-90-20

**2. CERAMIC PACKAGES**

**14-Pin Ceramic DIP Units: mm**

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B <sub>1</sub>	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	8.10	7.49
E <sub>1</sub>	7.82	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

**16-Pin Ceramic DIP Units: mm**

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B <sub>1</sub>	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E <sub>1</sub>	7.82	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

**20-Pin Ceramic DIP Units: mm**

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B <sub>1</sub>	1.14	1.52
C	0.20	0.38
D	25.78	26.33
E	8.10	8.60
E <sub>1</sub>	7.77	7.95
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

**24-Pin Ceramic DIP Units: mm**

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B <sub>1</sub>	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E <sub>1</sub>	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.776
S	1.85	1.93

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