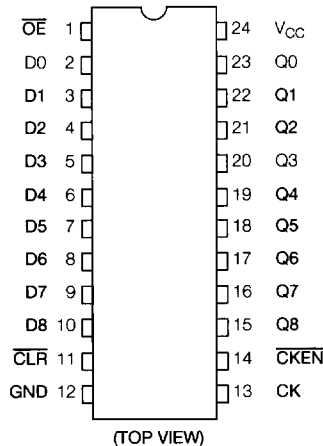


TC74ACT823 9-Bit D-Type Flip-Flop with 3-State Output

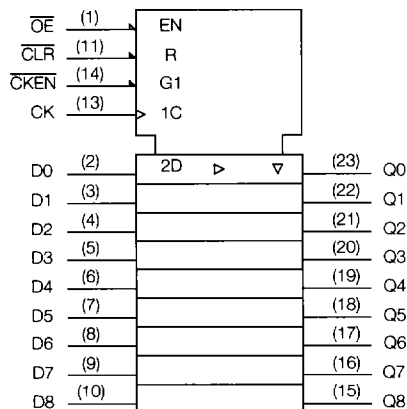
Features:

- **High Speed:** $f_{MAX} = 155\text{MHz}$ (typ.) at $V_{CC} = 5\text{V}$
- **Low Power Dissipation:** $I_{CC} = 8\mu\text{A}$ (max.) at $T_a = 25^\circ\text{C}$
- **Compatible with TTL Outputs:** $V_{IL} = 0.8\text{V}$ (max.); $V_{IH} = 2.0\text{V}$ (min.)
- **Symmetrical Output Impedance:** $I_{OH} = I_{OL} = 24\text{mA}$ (min.). Capability of driving 50Ω transmission lines.
- **Balanced Propagation Delays:** $t_{pLH} = t_{pHL}$
- **Pin and Function Compatible with 74F823**
- **Available in DIP Package**

Pin Assignment



IEC Logic Symbol



The TC74ACT823 is an advanced high speed CMOS 9-BIT BUS D-TYPE FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

This device can be used as a level converter for interfacing TTL input level of TTL or NMOS device to CMOS input level of Advanced High Speed CMOS.

The inputs can be connected to outputs of TTL, NMOS and CMOS devices directly.

The Clock (CK), Clock Enable ($\overline{\text{CKEN}}$), Clear ($\overline{\text{CLR}}$) and Output Enable ($\overline{\text{OE}}$) are common to all flip-flops.

When the $\overline{\text{CKEN}}$ is LOW, signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock signal.

With the $\overline{\text{CLR}}$ LOW all Q outputs are at low level independent of the other inputs.

When the $\overline{\text{OE}}$ is HIGH, the output go to the high impedance state.

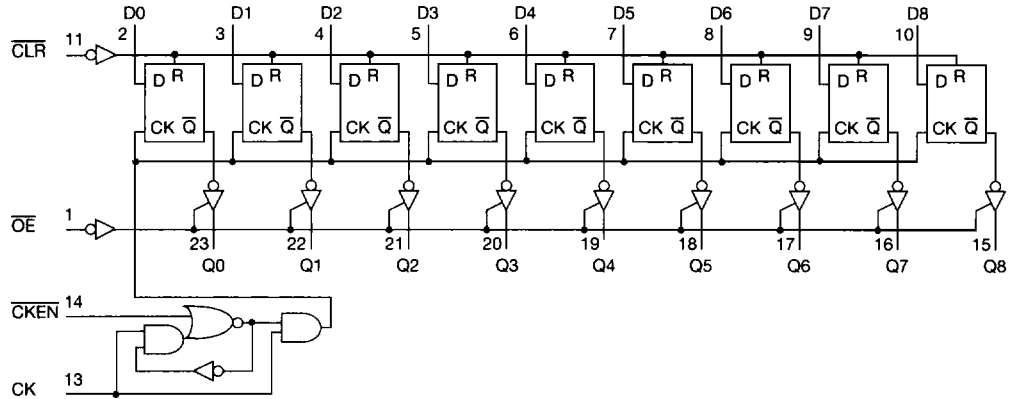
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Truth Table

INPUTS					OUTPUTS
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{CKEN}}$	CK	D	Q
L	L	X	X	X	L
L	H	L		H	H
L	H	L		L	L
L	H	H	X	X	Qn
H	X	X	X	X	Z

- X: Don't Care
Z: High Impedance
Q: No Change

System Diagram



Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5-7.0	V
DC Input Voltage	V_{IN}	$-0.5-V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5-V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 225	mA
Power Dissipation	P_D	500 (DIP) *	mW
Storage Temperature	T_{stg}	-65-150	$^{\circ}C$
Lead Temperature 10sec	T_L	300	$^{\circ}C$

* 500mW in the range of $T_a = -40^{\circ}C$ - $65^{\circ}C$.
From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ should be applied up to 300mW.

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5-5.5	V
Input Voltage	V_{IN}	$0-V_{CC}$	V
Output Voltage	V_{OUT}	$0-V_{CC}$	V
Operating Temperature	T_{opr}	-40-85	$^{\circ}C$
Input Rise and Fall Time	dt/dv	0-10	ns/v

DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION	V _{CC}	Ta = 25°C			Ta = -40-85°C		UNIT	
				Min.	Typ.	Max.	Min.	Max.		
High-Level Input Voltage	V _{IH}	—	4.5-5.5	2.0	—	—	2.0	—	V	
Low-Level Input Voltage	V _{IL}	—	4.5-5.5	—	—	0.8	—	0.8	V	
High-Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	4.5	4.4	4.5	—	4.4	—	V
			I _{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I _{OH} = -75mA*	5.5	—	—	—	3.85	—	
Low-Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I _{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I _{OL} = 75mA*	5.5	—	—	—	—	1.65	
3-State Output Off-State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5	—	—	±0.5	—	±5.0	μA	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	±0.1	—	±1.0		
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	8.0	—	80.0	mA	
	ΔI _{CC}	Per input: V _{CC} = 3.4V Other input: V _{CC} or GND	5.5	—	—	1.35	—	1.5		

* This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

Timing Requirements (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC}	Ta=25°C		Ta = -40-85°	UNIT
				Typ.	Max.	Max.	
Minimum Pulse Width (CK)	t _{w(H)} t _{w(L)}	—	5.0±0.5	—	5.0	5.0	ns
Minimum Pulse Width (CLR)	t _{w(L)}	—	5.0±0.5	—	5.0	5.0	
Minimum Set-up Time (DATA-CK)	t _s	—	5.0±0.5	—	3.0	3.0	
Minimum Set-up Time (CKEN-CK)	t _s	—	5.0±0.5	—	4.0	4.0	
Minimum Hold Time (DATA-CK)	t _h	—	5.0±0.5	—	2.0	2.0	
Minimum Hold Time (CKEN-CK)	t _h	—	5.0±0.5	—	3.0	3.0	
Minimum Removal Time (CLR)	t _{rem}	—	5.0±0.5	—	2.0	2.0	

AC Electrical Characteristics ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40-85°C		UNIT	
			V _{CC}	Min.	Typ.	Max.	Min.		Max.
Propagation Delay Time (CK-Q)	t _{pLH} t _{pHL}	—	5.0±0.5	—	7.1	11.0	1.0	12.5	ns
Propagation Delay Time (CLR-Q)	t _{pHL}	—	5.0±0.5	—	6.5	10.5	1.0	12.0	
Output Enable Time	t _{pZL} t _{pZH}	—	5.0±0.5	—	6.1	10.0	1.0	11.5	
Output Disable Time	t _{pLZ} t _{pHZ}	—	5.0±0.5	—	6.0	8.3	1.0	9.5	
Maximum Clock Frequency	f _{MAX}	—	5.0±0.5	90	140	—	80	—	MHz
Input Capacitance	C _{IN}	—	—	—	5	10	—	10	pF
Output Capacitance	C _{OUT}	—	—	—	10	—	—	—	
Power Dissipation Capacitance	C _{PD} ¹	—	—	—	47	—	—	—	

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC (opf)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 9$ (per F/F).

And the total C_{PD} when n pcs. of Flip-Flop operate can be gained by the following equation: $C_{PD} (total) = 35 + 12 \cdot n$.