

MM54HC374/MM74HC374



T-46-07-11

# MM54HC374/MM74HC374 TRI-STATE® Octal D-Type Flip-Flop

## General Description

These high speed Octal D-Type Flip-Flops utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

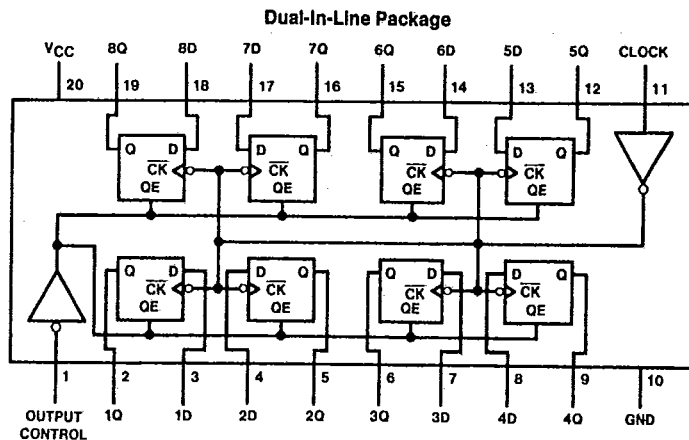
These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

## Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2-6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

## Connection Diagram



Top View

TL/F/5336-1

Order Number MM54HC374\* or MM74HC374\*

\*Please look into Section 8, Appendix D for availability of various package types.

## Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

H = high Level, L = Low Level  
 X = don't Care  
 ↑ = transition from low-to-high  
 Z = high impedance state  
 Q<sub>0</sub> = the level of the output before steady state input conditions were established

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### Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V <sub>CC</sub> )	-0.5 to +7.0V
DC Input Voltage (V <sub>IN</sub> )	-1.5 to V <sub>CC</sub> +1.5V
DC Output Voltage (V <sub>OUT</sub> )	-0.5 to V <sub>CC</sub> +0.5V
Clamp Diode Current (I <sub>IK</sub> , I <sub>OK</sub> )	±20 mA
DC Output Current, per pin (I <sub>OUT</sub> )	±35 mA
DC V <sub>CC</sub> or GND Current, per pin (I <sub>CC</sub> )	±70 mA
Storage Temperature Range (T <sub>STG</sub> )	-65°C to +150°C
Power Dissipation (P <sub>D</sub> ) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T <sub>L</sub> ) (Soldering 10 seconds)	260°C

### Operating Conditions

	Min	Max	Units
Supply Voltage (V <sub>CC</sub> )	2	6	V
DC Input or Output Voltage (V <sub>IN</sub> , V <sub>OUT</sub> )	0	V <sub>CC</sub>	V
Operating Temp. Range (T <sub>A</sub> )			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t <sub>r</sub> , t <sub>f</sub> )			
V <sub>CC</sub> =2.0V		1000	ns
V <sub>CC</sub> =4.5V		500	ns
V <sub>CC</sub> =6.0V		400	ns

### DC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub>	T <sub>A</sub> =25°C			Units	
				74HC		54HC		
				Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	V	
			4.5V	3.15	3.15	3.15	V	
			6.0V	4.2	4.2	4.2	V	
V <sub>IL</sub>	Maximum Low Level Input Voltage**		2.0V	0.5	0.5	0.5	V	
			4.5V	1.35	1.35	1.35	V	
			6.0V	1.8	1.8	1.8	V	
V <sub>OH</sub>	Minimum High Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	V	
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0 mA  I <sub>OUT</sub>   ≤ 7.8 mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
V <sub>OL</sub>	Maximum Low Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0V	0	0.1	0.1	V	
			4.5V	0	0.1	0.1	V	
			6.0V	0	0.1	0.1	V	
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0 mA  I <sub>OUT</sub>   ≤ 7.8 mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I <sub>IN</sub>	Maximum Input Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0V		±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum TRI-STATE Output Leakage Current	V <sub>IN</sub> =V <sub>IH</sub> , OC=V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND	6.0V		±0.5	±5	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ± 10% the worst case output voltages (V<sub>OH</sub> and V<sub>OL</sub>) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V<sub>IH</sub> and V<sub>IL</sub> occur at V<sub>CC</sub>=5.5V and 4.5V respectively. (The V<sub>IH</sub> value at 5.5V is 3.85V.) The worst case leakage current (I<sub>IN</sub>, I<sub>CC</sub>, and I<sub>OZ</sub>) occur for CMOS at the higher voltage and so the 6.0V values should be used.

\*\*V<sub>IL</sub> limits are currently tested at 20% of V<sub>CC</sub>. The above V<sub>IL</sub> specification (30% of V<sub>CC</sub>) will be implemented no later than Q1, CY'89.

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**AC Electrical Characteristics**  $V_{CC}=5V, T_A=25^{\circ}C, t_r=t_f=6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency		50	35	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Clock to Q	$C_L = 45\text{ pF}$	20	32	ns
$t_{PZH}, t_{PZL}$	Maximum Output Enable Time	$R_L = k\Omega$ $C_L = 45\text{ pF}$	19	28	ns
$t_{PHZ}, t_{PLZ}$	Maximum Output Disable Time	$R_L = k\Omega$ $C_L = 5\text{ pF}$	17	25	ns
$t_S$	Minimum Setup Time			20	ns
$t_H$	Minimum Hold Time			5	ns
$t_W$	Minimum Pulse Width		9	16	ns

**AC Electrical Characteristics**  $V_{CC}=2.0-6.0V, C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$  (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^{\circ}C$			Units	
				Typ	74HC $T_A = -40\text{ to }85^{\circ}C$	54HC $T_A = -55\text{ to }125^{\circ}C$		
$f_{MAX}$	Maximum Operating Frequency	$C_L = 50\text{ pF}$	2.0V		6	5	MHz	
			4.5V		30	24	MHz	
			6.0V		35	28	MHz	
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Clock to Q	$C_L = 50\text{ pF}$	2.0V	68	180	225	ns	
			2.0V	110	230	288	ns	
		$C_L = 150\text{ pF}$	4.5V	22	36	45	ns	
			4.5V	30	46	57	ns	
		$C_L = 50\text{ pF}$	6.0V	20	31	39	ns	
			6.0V	28	40	50	ns	
$t_{PZH}, t_{PZL}$	Maximum Output Enable Time	$R_L = 1\text{ k}\Omega$	2.0V	50	150	189	ns	
			2.0V	80	200	250	ns	
		$C_L = 50\text{ pF}$	4.5V	21	30	37	ns	
			4.5V	30	40	50	ns	
		$C_L = 150\text{ pF}$	6.0V	19	26	31	ns	
			6.0V	26	35	44	ns	
$t_{PHZ}, t_{PLZ}$	Maximum Output Disable Time	$R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$	2.0V	50	150	189	ns	
			4.5V	21	30	37	ns	
			6.0V	19	26	31	ns	
$t_S$	Minimum Setup Time		2.0V		50	60	ns	
			4.5V		9	13	ns	
			6.0V		9	11	ns	
$t_H$	Minimum Hold Time		2.0V		5	30	ns	
			4.5V		5	5	ns	
			6.0V		5	5	ns	
$t_W$	Minimum Pulse Width		2.0V	30	80	100	ns	
			4.5V	9	16	20	ns	
			6.0V	8	14	18	ns	
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time	$C_L = 50\text{ pF}$	2.0V	25	60	75	ns	
			4.5V	7	12	15	ns	
			6.0V	6	10	13	ns	
$t_r, t_f$	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	ns	
			4.5V		500	500	ns	
			6.0V		400	400	ns	
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per flip-flop) OC = $V_{CC}$ OC = GND		30			pF	
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

Note 5:  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .