INTEGRATED CIRCUITS

DATA SHEET

74LVC02Quad 2-input NOR gate

Product specification

1997 Feb 03

IC24 Data Handbook





Quad 2-input NOR gate

74LVC02

FEATURES

- Wide supply voltage: 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC02 is a high performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC02 provides the 2-input NOR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; t_{f} = t_{f} \leq 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} t _{PLH}	Propagation delay nA, nB to nY	$C_L = 50 \text{ pF};$ $V_{CC} = 3.3 \text{ V}$	3.3	ns
C _I	Input capacitance		5.0	pF
C _{PD}	Power dissipation capacitance per gate	Notes 1 and 2	60	pF

NOTES:

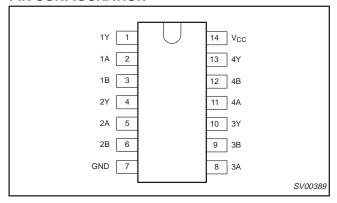
- 1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 - $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 - f_i = input frequency in MHz; C_L = output load capacity in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V;

 - $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of the outputs.}$
- 2. The condition is $V_I = GND$ to V_{CC} .

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVC02 D	74LVC02 D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC02 DB	74LVC02 DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC02 PW	74LVC02PW DH	SOT402-1

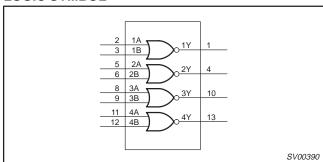
PIN CONFIGURATION



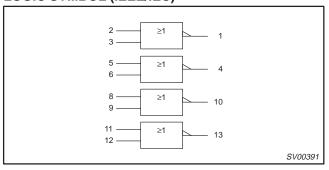
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y – 4Y	Data outputs
2, 5, 8, 11	1A – 4A	Data inputs
3, 6, 9, 12	1B – 4B	Data inputs
7	GND	Ground (0 V)
14	V _{CC}	Positive supply voltage

LOGIC SYMBOL



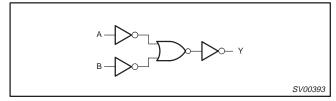
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM (ONE GATE)



FUNCTION TABLE

INP	OUTPUTS	
nA	nB	nY
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

NOTES:

H = HIGH voltage level L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIM	UNIT		
STWIBOL	TANAMETER	CONDITIONS	MIN	MAX	0	
V _{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V	
V _{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V	
VI	DC input voltage range		0	5.5	V	
V _{I/O}	DC input voltage range for I/Os		0	V _{CC}	V	
Vo	DC output voltage range		0	V _{CC}	V	
T _{amb}	Operating free-air temperature range		-40	+85	°C	
t _r , t _f	Input rise and fall times	$V_{CC} = 1.2 \text{ to } 2.7V$ $V_{CC} = 2.7 \text{ to } 3.6V$	0	20 10	ns/V	

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +6.5	V
I _{IK}	DC input diode current	$V_I < 0$	-50	mA
VI	DC input voltage	Note 2	-0.5 to +5.5	V
V _{I/O}	DC input voltage range for I/Os		-0.5 to V _{CC} +0.5	V
I _{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V _{OUT}	DC output voltage	Note 2	-0.5 to V _{CC} +0.5	V
I _{OUT}	DC output source or sink current	$V_O = 0$ to V_{CC}	±50	mA
I _{GND} , I _{CC}	DC V _{CC} or GND current		±100	mA
T _{stg}	Storage temperature range		-60 to +150	°C
P _{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

			L	UNIT		
SYMBOL	PARAMETER	TEST CONDITIONS	Temp = -			
			MIN	TYP ¹	MAX	
V	HICH level Input voltege	V _{CC} = 1.2V	V _{CC}			V
V _{IH}	HIGH level Input voltage	V _{CC} = 2.7 to 3.6V	2.0			ľ
	LOW lovel land voltage	V _{CC} = 1.2V			GND	V
V _{IL}	LOW level Input voltage	V _{CC} = 2.7 to 3.6V			0.8	V
		$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -12mA$	V _{CC} - 0.5			
	HIGH level output voltage	$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -100\mu A$	V _{CC} - 0.2	V _{CC}		V
V _{OH}		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -12mA$	V _{CC} -0.6			
		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -24$ mA	V _{CC} - 1.0			
	LOW level output voltage	$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = 12mA$			0.40	
V _{OL}		$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL}; I_O = 100 \mu A$		GND	0.20	\ \
		$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL;} I_O = 24\text{mA}$			0.55	1
l _l	Input leakage current	$V_{CC} = 3.6V$; $V_I = 5.5V$ or GND Not for I/O pins		±0.1	±5	μΑ
I _{IHZ} /I _{ILZ}	Input current for common I/O pins	$V_{CC} = 3.6V$; $V_I = V_{CC}$ or GND		±0.1	±15	μΑ
l _{OZ}	3-State output OFF-state current	$V_{CC} = 3.6V$; $V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND		0.1	±10	μΑ
Icc	Quiescent supply current	$V_{CC} = 3.6V; V_I = V_{CC} \text{ or GND}; I_O = 0$		0.1	20	μΑ
Δl _{CC}	Additional quiescent supply current per input pin	$V_{CC} = 2.7V \text{ to } 3.6V; V_I = V_{CC} - 0.6V; I_O = 0$		5	500	μА

NOTE:

AC CHARACTERISTICS

GND = 0 V; t_r = $t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500 Ω ; T_{amb} = -40°C to +85°C

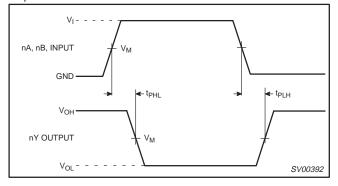
			LIMITS							
SYMBO PARAMETER		WAVEFORM	$V_{CC} = 3.3V \pm 0.3V$		V _{CC} = 2.7V		V _{CC} = 1.2V	UNIT		
			MIN	TYP ¹	MAX	MIN	TYP ¹	MAX	TYP	
t _{PHL} /t _{PLH}	Propagation delay nA, nB to nY	Figures 1, 2	1.5	3.5	6.0	1.5	4.0	6.5	20	ns

NOTE:

AC WAVEFORMS

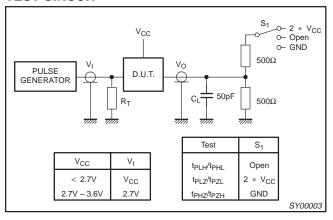
 V_{M} = 1.5 V at $V_{CC} \ge 2.7$ V V_{M} = 0.5 • V_{CC} at $V_{CC} < 2.7$ V

 $V_{\mbox{\scriptsize OL}}$ and $V_{\mbox{\scriptsize OH}}$ are the typical output voltage drop that occur with the output load.



Waveform 1. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT



Waveform 2. Load circuitry for switching times.

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^{1.} All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

^{1.} These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

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DEFINITIONS					
Data Sheet Identification	Product Status	Definition			
Objective Specification	Objective Specification Formative or in Design This data sheet contains the design target or goal specifications for product development. If may change in any manner without notice.				
Preliminary Specification Preproduction Product		This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.			
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