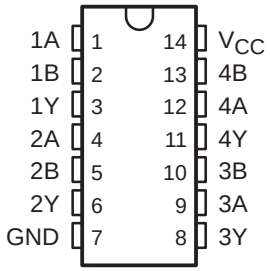
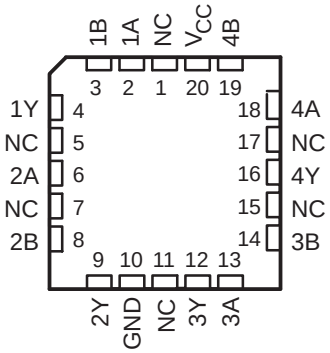
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPS**

SN54ACT32 . . . J OR W PACKAGE
SN74ACT32 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54ACT32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

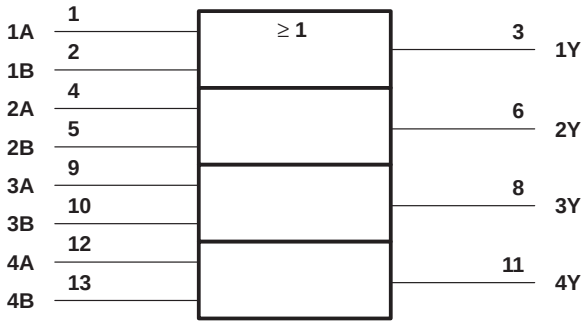
The ’ACT32 are quadruple 2-input positive-OR gates. The devices perform the Boolean function $Y = A + B$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

The SN54ACT32 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(EACH GATE)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



logic diagram (positive logic)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package . . . . . 1.25 W
DB package . . . . . 0.5 W
N package . . . . . 1.1 W
PW package . . . . . 0.5 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ACT32		SN74ACT32		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	8	0	8	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54ACT32		SN74ACT32		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = –24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I_{OH} = –50 mA†	5.5 V				3.86				
	I_{OH} = –75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V		0.001	0.1		0.1		0.1	V
		5.5 V		0.001	0.1		0.1		0.1	
	I_{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		40		20	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V		0.6			1.6		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5 V		2.6						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

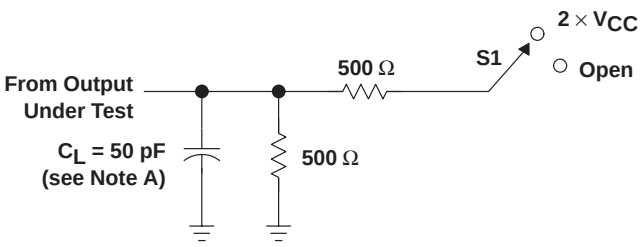
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54ACT32		SN74ACT32		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1	6.5	9			1	10	ns
t_{PHL}			1	6.5	9			1	10	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

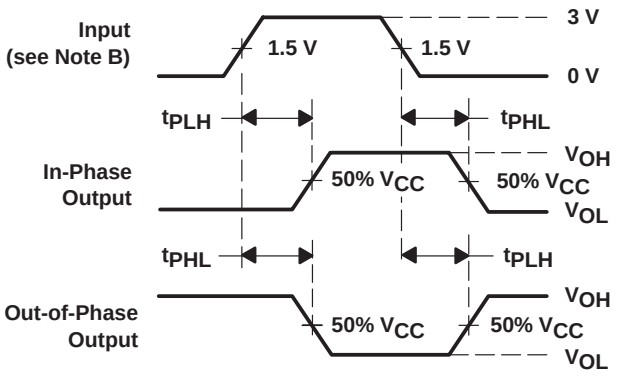
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	40	pF

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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SN74ACT32, Quadruple 2-Input Positive-OR Gates

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74ACT32
Voltage Nodes (V)	5
Output Level	CMOS
Static Current	0.02

FEATURES

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- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPS

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DESCRIPTION

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The 'ACT32 are quadruple 2-input positive-OR gates. The devices perform the Boolean function Y = A + B or Y = A\ • B\ in positive logic.

The SN54ACT32 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ACT32 is characterized for operation from -40°C to 85°C.

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74act32.pdf (89 KB,Rev.A) (Updated: 05/01/1996)

APPLICATION NOTES

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View Application Notes for Digital Logic

- CMOS Power Consumption and CPD Calculation (Rev. B) (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES Back to Top

ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74ACT32D	SOP (D)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ACT32DBR	SSOP (DB)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ACT32N	PDIP (N)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ACT32PWR	TSSOP (PW)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG Back to Top

DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74ACT32D	ACTIVE	SOP (D) | 14	-40 TO 85	View Contents	1KU | 0.20	50	N/A*	8450 | 03 Oct	8 WKS	Avnet | AMERICA	>1k	BUY NOW
										DigiKey | AMERICA	>1k	BUY NOW
SN74ACT32DBLE	OBSOLETE	SSOP (DB) | 14	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74ACT32DBR	ACTIVE	SSOP (DB) | 14	-40 TO 85	View Contents	1KU | 0.20	2000	N/A*	1031 | 23 Sep	8 WKS			
								969 | 12 Nov				
SN74ACT32DR	ACTIVE	SOP (D) | 14	-40 TO 85	View Contents	1KU | 0.20	2500	N/A*	2346 | 02 Oct	8 WKS	Avnet | AMERICA	>1k	BUY NOW
								154 | 03 Oct		DigiKey | AMERICA	>1k	BUY NOW
SN74ACT32N	ACTIVE	PDIP (N) | 14	-40 TO 85	View Contents	1KU | 0.20	25	N/A*	7 | 23 Sep	6 WKS	Avnet | AMERICA	253	BUY NOW
								>10k | 02 Oct				
								>10k | 08 Oct				
SN74ACT32NSR	ACTIVE	SOP (NS) | 14		View Contents	1KU | 0.21	2000	N/A*	1421 | 23 Sep	8 WKS			
SN74ACT32PWLE	OBSOLETE	TSSOP (PW) | 14	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74ACT32PWR	ACTIVE	TSSOP (PW) | 14	-40 TO 85	View Contents	1KU | 0.20	2000	N/A*	1923 | 25 Sep	8 WKS			

- IBIS Model of SN74ACT32 (SCAM031, 78 KB - Updated: 09/05/2002)
  IBIS Model of SN74ACT32 (SCAM031, 15 KB, ZIP - Updated: 09/05/2002)

Table Data Updated on: 9/26/2002