National Semiconductor

MM54HCT540/MM74HCT540 Inverting Octal TRI-STATE® Buffer MM54HCT541/MM74HCT541 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize advanced silicon-gate CMOS technology and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. Both devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM54HCT540/MM74HCT540 is an inverting buffer and the MM54HCT541/MM74HCT541 is a non-inverting buffer. The TRI-STATE control gate operates as a two-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

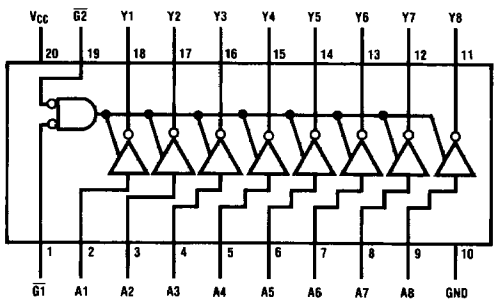
In order to enhance PC board layout, the 'HCT540 and 'HCT541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Low quiescent current: 80 μA
- Output current: 6 mA (min.)

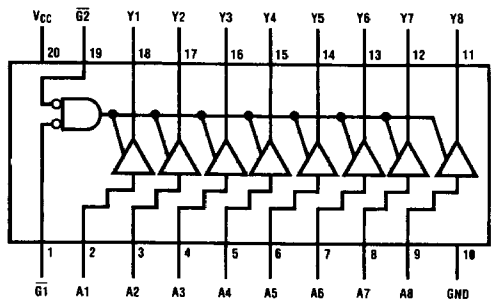
Connection Diagrams

Dual-In-Line Package



TL/F/6040–1

Top View



TL/F/6040–2

Top View

Order Number MM54HCT540* or MM74HCT540*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or GND.

AC Electrical Characteristics MM54HCT540/MM74HCT540

V_{CC} = 5.0V, t_r = t_f = 6 ns, T_A = 25°C, (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	12	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF R_L = 1 kΩ	14	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF R_L = 1 kΩ	13	25	ns

AC Electrical Characteristics MM54HCT540/MM74HCT540

$V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions		$T_A = 25°C$	74HCT $T_A = -40$ to $85°C$		54HCT $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 50$ pF		12	20	25	30	ns
		$C_L = 150$ pF		22	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ	$C_L = 50$ pF	15	30	38	45	ns
			$C_L = 150$ pF	20	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 50$ pF		15	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G} = V_{CC}$ $\overline{G} = GND$	12 50				pF pF

AC Electrical Characteristics MM54HCT541/MM74HCT541

$V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $T_A = 25°C$, (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 45$ pF	13	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L = 45$ pF $R_L = 1$ kΩ	17	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L = 5$ pF $R_L = 1$ kΩ	15	25	ns

AC Electrical Characteristics MM54HCT541/MM74HCT541

$V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions		$T_A = 25°C$	74HCT $T_A = -40$ to $85°C$		54HCT $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 50$ pF		14	23	29	34	ns
		$C_L = 150$ pF		17	33	42	49	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ	$C_L = 50$ pF	17	30	38	45	ns
			$C_L = 150$ pF	22	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 50$ pF		17	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G} = V_{CC}$ $\overline{G} = GND$	12 45				pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.