

## **SN5474, SN54H74, SN54L74, SN54LS74A, SN54S74 SN7474, SN74H74, SN74LS74A, SN74S74**

### *Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear*

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

#### **Rochester Electronics Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

#### **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

# TYPES SN5474, SN54H74, SN54L74, SN54LS74A, SN54S74, SN7474, SN74H74, SN74LS74A, SN74S74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN5474, SN54H74, SN54L74 ... J PACKAGE  
SN54LS74A, SN54S74 ... J OR W PACKAGE  
SN7474, SN74H74 ... J OR N PACKAGE  
SN74LS74A, SN74S74 ... D, J OR N PACKAGE

### description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

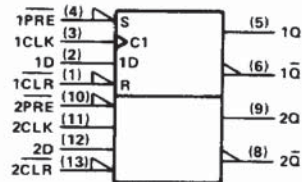
The SN54' family is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74' family is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

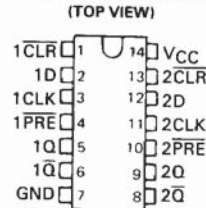
INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

<sup>†</sup> The output levels in this configuration are not guaranteed to meet the minimum levels in  $V_{OH}$  if the lows at preset and clear are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

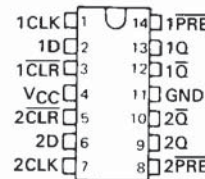
### logic symbol



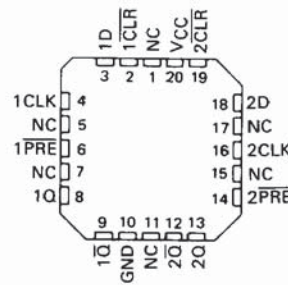
Pin numbers shown on logic notation are for D, J or N packages.



SN5474, SN54H74 ... W PACKAGE  
(TOP VIEW)

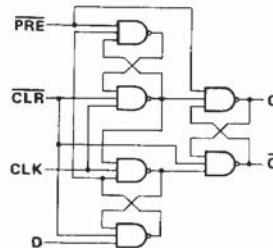


SN54LS74A, SN54S74 ... FK PACKAGE  
SN74LS74A, SN74S74 ... FN PACKAGE  
(TOP VIEW)



NC - No internal connection

### logic diagram



**PRODUCTION DATA**  
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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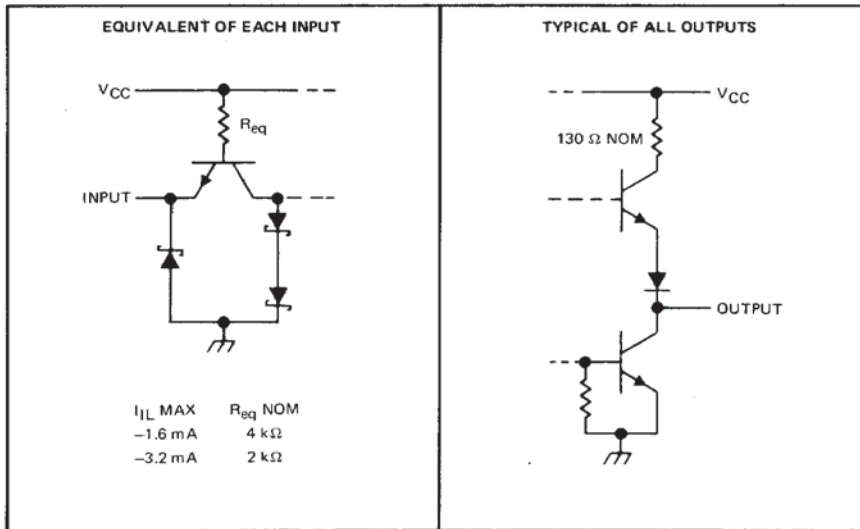
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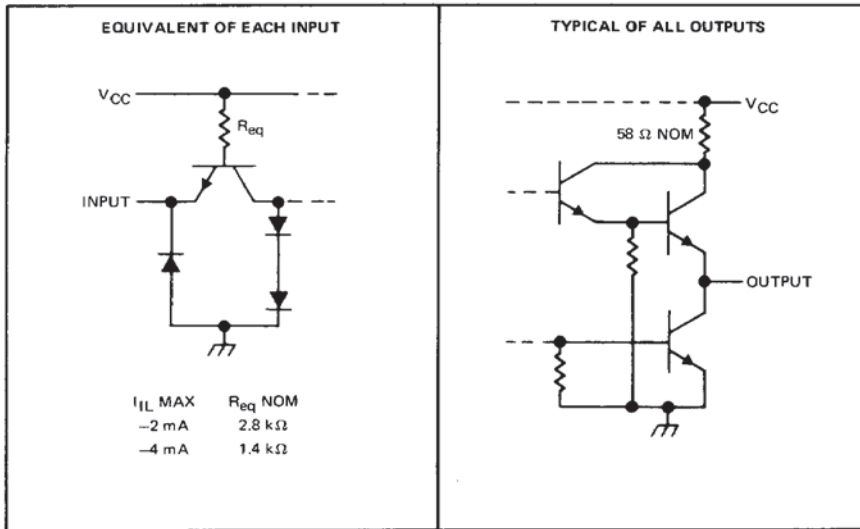
TYPES SN5474, SN54H74, SN7474, SN74H74  
 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

schematics of inputs and outputs

74



'H74

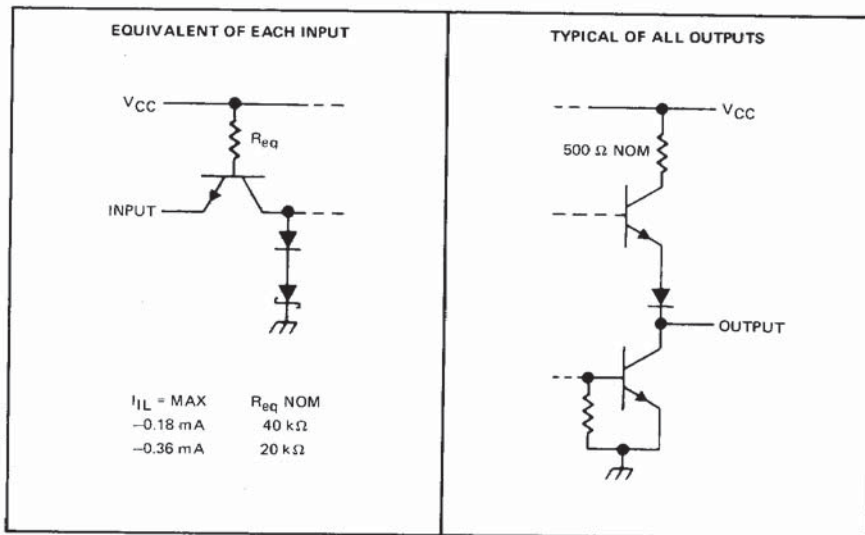


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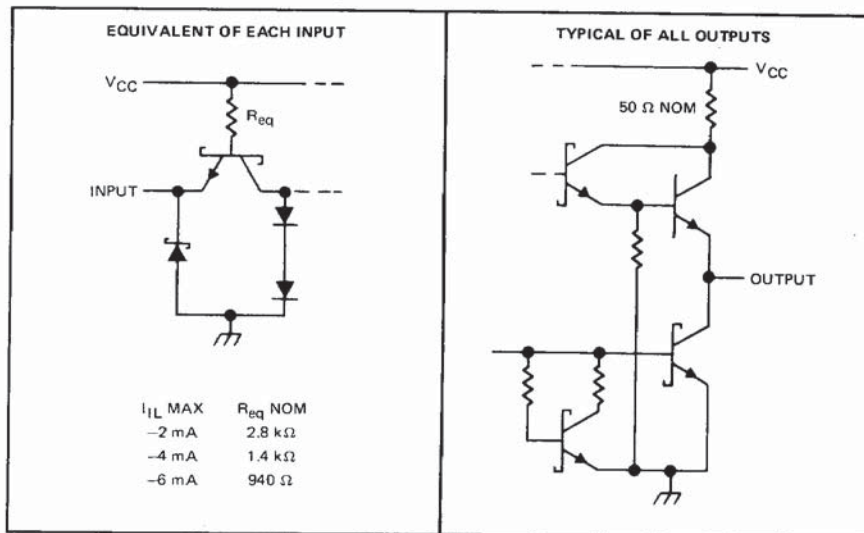
TYPES SN54L74, SN54S74, SN74S74  
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

schematics of inputs and outputs (continued)

'L74



'S74

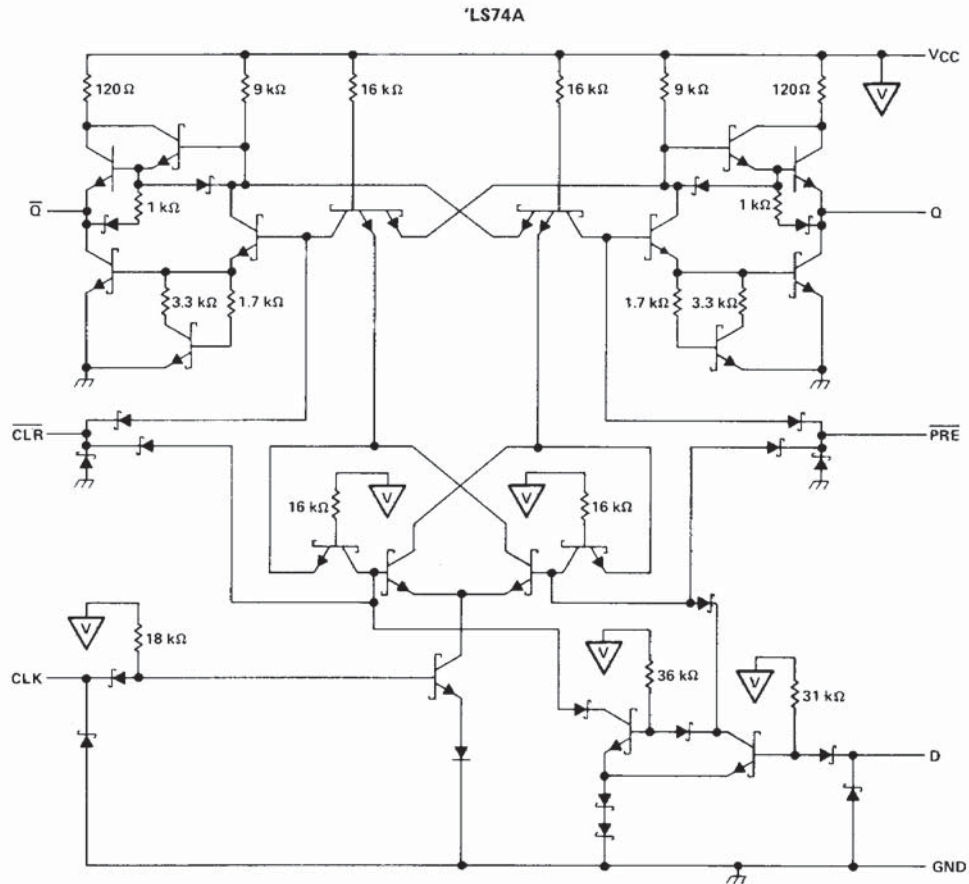


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TYPES SN5474, SN54H74, SN54L74, SN54LS74A, SN54S74,  
 SN7474, SN74H74, SN74LS74A, SN74S74  
 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

schematic



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: '74, 'H74, 'L74, 'S74	5.5 V
'LS74A	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN5474, SN7474

**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

**recommended operating conditions**

	SN5474			SN7474			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
I <sub>OH</sub> High-level output current			-0.4			-0.4	mA
I <sub>OL</sub> Low-level output current			16			16	mA
t <sub>w</sub> Pulse duration	CLK high	30		30			ns
	CLK low	37		37			
	PRE or CLR low	30		30			
t <sub>SU</sub> Input setup time before CLK †	20			20			ns
t <sub>H</sub> Input hold time-data after CLK †	5			5			ns
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN5474			SN7474			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -0.4 mA, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V	2.4	3.4		2.4	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 16 mA, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V		0.2	0.4		0.2	0.4	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	D			40			40	mA
	CLR			120			120	
	All Other	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V		80			80	
I <sub>IL</sub>	D			-1.6			-1.6	mA
	PRE*			-1.6			-1.6	
	CLR*			-3.2			-3.2	
	CLK	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-3.2			-3.2	
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-20		-57	-18		-57	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See Note 2		8.5	15		8.5	15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

\* Clear is tested with preset high and preset is tested with clear high.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>				15	25		MHz
t <sub>PLH</sub>	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\bar{Q}$	R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF			25	ns
t <sub>PHL</sub>						40	ns
t <sub>PLH</sub>	CLK	Q or $\bar{Q}$			14	25	ns
t <sub>PHL</sub>					20	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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**TYPES SN54H74, SN74H74**  
**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

**recommended operating conditions**

		SN54H74			SN74H74			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
V <sub>IH</sub>	High-level input voltage	2			2			V	
V <sub>IL</sub>	Low-level input voltage				0.8			V	
I <sub>OH</sub>	High-level output current				-1			mA	
I <sub>OL</sub>	Low-level output current				20			mA	
t <sub>w</sub>	Pulse duration	CLK high		15	15		ns		
		CLK low		13.5	13.5				
		CLR or PRE low		25	25				
t <sub>su</sub>	Setup time-before CLK †	High-level data		10	10		ns		
		Low-level data		15	15				
t <sub>h</sub>	Hold time - data after CLK †	5			5			ns	
T <sub>A</sub>	Operating free-air temperature	-55			125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN54H74			SN74H74			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -8 mA	-1.5			-1.5			V	
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA	2.4	3.4		2.4	3.4		V	
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA	0.2	0.4		0.2	0.4		V	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1			1			mA	
I <sub>IH</sub>	D	50			50			µA	
	CLR	150			150				
	PRE or CLK	100			100				
I <sub>IL</sub>	D	-2			-2			mA	
	CLR*	-4			-4				
	PRE*	-2			-2				
	CLK	-4			-4				
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-40	-100		-40	-100		mA	
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See Note 2	15			21	15		25	mA

- † For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.  
 ‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.  
 § Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.  
 \* Clear is tested with preset high and preset is tested with clear high.  
 NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
f <sub>max</sub>				35	43		MHz	
t <sub>PLH</sub>	PRE or CLR	Q or Q̄	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 25 pF	20			ns	
t <sub>PHL</sub>				30			ns	
t <sub>PLH</sub>	CLK	Q or Q̄		8.5			15	ns
t <sub>PHL</sub>				13			20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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# TYPE SN54L74

## DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

### recommended operating conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.7	V
I <sub>OH</sub>	High-level output current			-0.1	mA
I <sub>OL</sub>	Low-level output current			2	mA
t <sub>w</sub>	Pulse duration	CLK high or low		200	ns
		CLR or PRE low		100	
t <sub>su</sub>	Setup time before CLK †	50			ns
t <sub>h</sub>	Hold time data after CLK †	15			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †				MIN	TYP ‡	MAX	UNIT
V <sub>OH</sub>	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,	V <sub>IL</sub> = 0.7 V,	I <sub>OH</sub> = -0.1 mA	2.4	3.3		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,	V <sub>IL</sub> = 0.7 V,	I <sub>OL</sub> = 2 mA	0.15	0.3		V
I <sub>I</sub>	D	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			0.1		mA	
	CLR				0.3			
	PRE or CLK				0.2			
I <sub>IH</sub>	D	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			10		μA	
	CLR				30			
	PRE or CLK				20			
I <sub>IL</sub>	D or PRE	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.3 V			-0.18		μA	
	CLR or CLK				-0.36			
I <sub>OS</sub>	V <sub>CC</sub> = MAX				-3	-15		mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See Note 2					0.8	1.5	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f <sub>max</sub>					2.5	3		MHz
t <sub>PLH</sub>	PRE or CLR	Q or Q̄	R <sub>L</sub> = 4 kΩ, C <sub>L</sub> = 50 pF		50	75		ns
t <sub>PHL</sub>	PRE or CLR (CLK high)				80	150		ns
					80	150		
t <sub>PLH</sub>	Clock	Q or Q̄			15	65	100	ns
t <sub>PHL</sub>					15	65	150	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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**TYPES SN54LS74A, SN74LS74A**  
**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

**recommended operating conditions**

		SN54LS74A			SN74LS74A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage	0.7			0.8			V
I <sub>OH</sub>	High-level output current	-0.4			-0.4			mA
I <sub>OL</sub>	Low-level output current	4			8			mA
f <sub>clock</sub>	Clock frequency	0			25			MHz
t <sub>w</sub>	Pulse duration	CLK high	25		25		ns	
		PRE or CLR low	25		25			
t <sub>su</sub>	Setup time-before CLK †	High-level data	20		20		ns	
		Low-level data	20		20			
t <sub>h</sub>	Hold time-data after CLK †	5			5			ns
T <sub>A</sub>	Operating free-air temperature	-55			125			°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN54LS74A		SN74LS74A		UNIT
		MIN	TYP‡	MAX	MIN	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.5				V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4 mA	2.5	3.4	2.7	3.4	V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 4 mA, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V,	0.25	0.4	0.25	0.4	V
	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 8 mA, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V,	0.35 0.5				
I <sub>I</sub>	D or CLK	0.1				mA
	CLR or PRE	0.2				
I <sub>IH</sub>	D or CLK	20				µA
	CLR or PRE	40				
I <sub>IL</sub>	D or CLK	-0.4				mA
	CLR or PRE	-0.8				
I <sub>OS</sub> §	V <sub>CC</sub> = MAX, See Note 4	-20	-100	-20	-100	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See Note 2	4	8	4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>			R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF	25	33		MHz
t <sub>PLH</sub>	CLR, PRE or CLK	Q or $\bar{Q}$		13	25		ns
t <sub>PHL</sub>				25	40		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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**TTL DEVICES**

TYPES SN54S74, SN74S74

**DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR**

**recommended operating conditions**

	SN54S74			SN74S74			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage	0.8			0.8			V
I <sub>OH</sub> High-level output current	-1			-1			mA
I <sub>OL</sub> Low-level output current	20			20			mA
t <sub>w</sub> Pulse duration	CLK high	6		6		ns	
	CLK low	7.3		7.3			
	CLR or PRE low	7		7			
t <sub>su</sub> Setup time, before CLK †	High-level data	3		3		ns	
	Low-level data	3		3			
t <sub>h</sub> Input hold time - data after CLK †	2		2		ns		
T <sub>A</sub> Operating free-air temperature	-55		125		0 70		°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN54S74		SN74S74		UNIT
		MIN	TYP‡	MAX	MIN	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA,			-1.2		V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA	2.5	3.4	2.7	3.4	V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA	0.5		0.5		V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1		1		mA
I <sub>IH</sub>	D	50		50		mA
	CLR	150		150		
	PRE or CLK	100		100		
I <sub>IL</sub>	D	-2		-2		mA
	CLR*	-6		-6		
	PRE*	-4		-4		
	CLK	-4		-4		
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-40	-100	-40	-100	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See Note 2	15	25	15	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

\* Clear is tested with preset high and preset is tested with clear high.

NOTE 2: All outputs open, I<sub>CC</sub> is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>				75	110		MHz
t <sub>PLH</sub>	PRE or CLR	Q or Q̄	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF	4	6		ns
t <sub>PHL</sub>	PRE or CLR (CLK high)	Q̄ or Q		9	13.5		ns
	PRE or CLR (CLK low)	Q or Q̄		5	8		
t <sub>PLH</sub>	CLK	Q or Q̄		6	9		ns
t <sub>PHL</sub>				6	9		

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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TTL DEVICES