Am2919

Quad Register with Dual Three-State Outputs

DISTINCTIVE CHARACTERISTICS

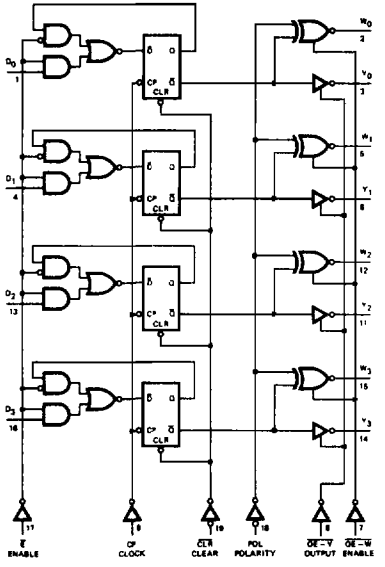
- Four D-type flip-flops
- Two sets of three-state outputs
- Polarity control on one set of outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs

GENERAL DESCRIPTION

The Am2919 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs—W and Y—are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am2919 is packaged in a space-saving (0.3-inch row spacing) 20-pin package.

BLOCK DIAGRAM



BD002400

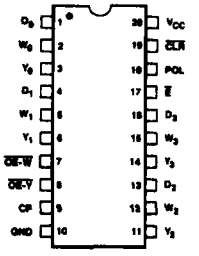
RELATED PRODUCTS

Part No.	Description
Am25LS2519	Quad Register
Am25LS2518	Quad D Register

03597B

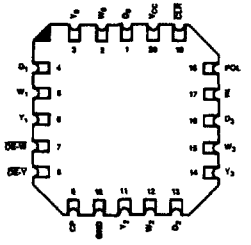
CONNECTION DIAGRAM
Top View

P-20
D-20
F-20*



CD004590

L-20-1



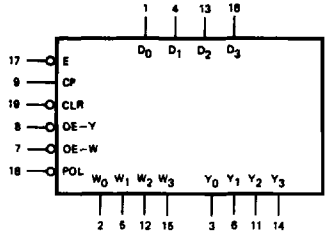
CD004600

*F-20 pin configuration identical to D-20, P-20.

Note: Pin 1 is marked for orientation

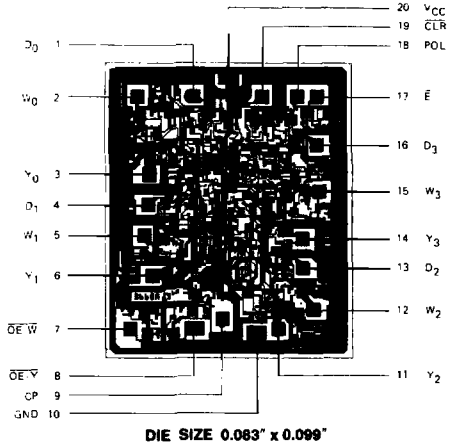
5

LOGIC SYMBOL



LS001000

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.083" x 0.099"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2919 **D** **C** **B**

- B — Screening Option: Blank – Standard processing; B – Burn-in
- C — Temperature (See Operating Range): C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D – 20-pin CERDIP; F – 20-pin flatpak; L – 20-pin leadless chip carrier; P – 20-pin plastic DIP; X – Dice

Device type: Quad Register

Valid Combinations	
Am2912	PC DC, DCB, DM, DMB FM, FMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

03597B

Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

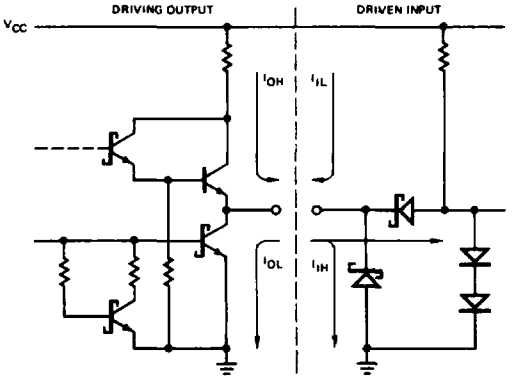
Pin No.	Name	I/O	Description
1, 4, 13, 16	D_i	I	Any of the four D flip-flop data lines.
17	$\overline{E}$	I	Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.
9	CP	I	Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.
7, 8	$\overline{OE}$-W, $\overline{OE}$-Y	I	Output Enable. When $\overline{OE}$ is LOW, the register is enabled to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE}$-W controls the W set of outputs, and $\overline{OE}$-Y controls the Y set.
3, 6, 11, 14	Y_i	O	Any of the four non-inverting three-state output lines.
2, 5, 12, 15	W_i	O	Any of the four three-state outputs with polarity control.
18	POL	I	Polarity Control. The W_i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.
19	$\overline{CLR}$	I	Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/ Output	Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	D_0	1.0	–	–	–	–
2	W_0	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	D_1	1.0	–	–	–	–
5	W_1	–	50	130	33	33
6	Y_1	–	50	130	33	33
7	$\overline{OE}$–W	1.0	–	–	–	–
8	$\overline{OE}$–Y	1.0	–	–	–	–
9	CP	1.0	–	–	–	–
10	GND	–	–	–	–	–
11	Y_2		50	130	33	33
12	W_2		50	130	33	33
13	D_2	1.0	–	–	–	–
14	Y_3	–	50	130	33	33
15	W_3	–	50	130	33	33
16	D_3	1.0	–	–	–	–
17	$\overline{E}$	1.0	–	–	–	–
18	POL	1.0	–	–	–	–
19	$\overline{CLR}$	1.0	–	–	–	–
20	V_{CC}	–	–	–	–	–

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

Note: Actual current flow direction shown.

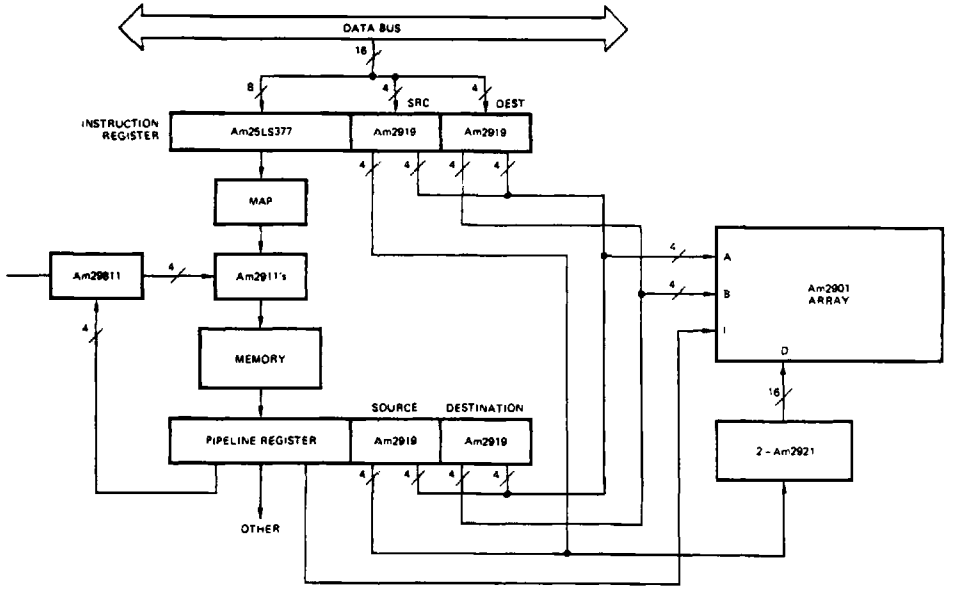
FUNCTION TABLE

Function	Inputs							Internal	Outputs	
	CP	D_I	$\overline{E}$	$\overline{CLR}$	POL	$\overline{OE}$-W	$\overline{OE}$-Y	Q	W_I	Y_I
Output Three-State Control	X X X X	X X X X	X X X X	X X X X	X X X X	H L H L	L H H L	NC NC NC NC	Z Enabled Z Enabled	Enabled Z Z Enabled
W_i Polarity	X X	X X	X X	X X	L H	L L	L L	NC NC	Non-Inverting Inverting	Non-Inverting Non-Inverting
Asynchronous Clear	X X	X X	X X	L L	L H	L L	L L	L L	L H	L L
Clock Enabled	↑ ↑ ↑ ↑ ↑	X L L H H	H L L L L	H H H H H	X L H L H	X L L L L	X L L L L	NC L L H H	NC L H H L	NC L L H H

L = LOW
H = HIGH
Z = High Impedance
NC = No Change
X = Don't Care
↑ = LOW-to-HIGH Transition

5

APPLICATION



AF001850

The Am2919 provides for easy control of the selection of source and destination register addresses for the Am2901. These controls can emanate from both the instruction register and the pipeline register. The control is accomplished by three-state action at the Am2919 outputs. Four different register outputs can be selected by the B address which is the destination register in the Am2901. Two registers can be selected for the Am2901 A input which is a second RAM source.

The other pair of three-state outputs can be used for function control select as shown with the Am2921. Here, bit set, bit clear, bit toggle and bit test on any of the 16 bits can be performed.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_H or V_{IL}	MIL, I_{OH} = −1.0mA		2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 7.0V					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V				−20	μA
			V_O = 2.4V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX		MIL		24	36	mA
				COM'L		24	39	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded: outputs open.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{PHL}	Clock to Y_i		C_L = 15pF R_L = 2.0kΩ		22	33	ns
t_{PHL}					20	30	
t_{PLH}	Clock to W_i (Either Polarity)				24	36	ns
t_{PHL}					24	36	
t_{PHL}	Clear to Y_i				29	43	ns
t_{PLH}	Clear to W_i				25	37	ns
t_{PHL}					30	45	
t_{PLH}	Polarity to W_i				23	34	ns
t_{PHL}					25	37	
t_{pw}	Clear			18			ns
t_{pw}	Clock Pulse Width	LOW		15			ns
		HIGH		18			
t_s	Data			15			ns
t_h	Data			5			ns
t_s	Data Enable			20			ns
t_h	Data Enable			0			ns
t_s	Set-up Time, Clear Recovery (Inactive) to Clock			20	15		ns
t_{ZH}	Output Enable to W or Y				11	17	ns
t_{ZL}					13	20	
t_{HZ}	Output Enable to W or Y		C_L = 5.0pF R_L = 2.0kΩ		13	20	ns
t_{LZ}					11	17	
f_{max}	Maximum Clock Frequency (Note 1)		C_L = 15pF R_L = 2.0kΩ	35	45		MHz

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

				Commercial		Military		
				Am2919		Am2919		
Parameters	**Description**		**Test Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{PLH}	Clock to Y_i		C_L = 50pF R_L = 2.0kΩ		39		42	ns
t_{PHL}					39		45	
t_{PLH}	Clock to W_i (Either Polarity)				41		43	ns
t_{PHL}					44		48	
t_{PHL}	Clear to Y_i				52		58	ns
t_{PLH}	Clear to W_i				42		43	ns
t_{PHL}					51		53	
t_{PLH}	Polarity to W_i				41		45	ns
t_{PHL}					42		44	
t_{pw}	Clear			20		20		ns
t_{pw}	Clock	LOW		20		20		ns
		HIGH		20		20		
t_s	Data			15		15		ns
t_h	Data			10		10		ns
t_s	Data Enable			25		25		ns
t_h	Data Enable			0		0		ns
t_s	Set-up Time, Clear Recovery (Inactive) to Clock			23		24		ns
t_{ZH}	Output Enable to W_i or Y_i				24		27	ns
t_{ZL}					29		35	
t_{HZ}	Output Enable to W_i or Y_i		C_L = 5.0pF R_L = 2.0kΩ		33		45	ns
t_{LZ}					22		26	
f_{max}	Maximum Clock Frequency (Note 1)		C_L = 50pF R_L = 2.0kΩ	30		25		MHz

*Switching Characteristics' performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.