PLESSEY Semiconductors — ADVANCE INFORMATION CMOS

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MV4311 MV4368 MV4511

LATCHED 7-SEGMENT DECODER/DRIVERS

The MV4311, MV4368 and MV4511 are latched 7-Segment Decoder/Drivers fabricated with the Metal Gate CMOS Process and feature Bipolar NPN output stages sourcing well in excess of 20mA per segment output. Therefore current limiting resistors (e.g. 150-270 ohms) should be utilised when direct driving LED displays.

Latches on the four Address (Data) inputs (A,B,C,D) are controlled by Latch Enable (LE). When LE is low the output state is determined by the input data (Fallthrough). When LE is taken high that data at the inputs satisfying the setup time is stored in the latches and the outputs remain stable (Latch enabled). The high impedance of the data inputs permits direct multiplexed drive from MOS devices without need for additional drivers.

The MV4511 contains a BCD-to-7-segment decoder which blanks the outputs (all low) on input codes 10 through 15. The MV4311 and MV4368 contain a Hexadecimal-to-7-segment decoder producing numeric output 0 through 9 and alpha output, using mixed upper and lower case, A through F, as shown in Fig. 2.

The MV4311 and MV4511 also include Lamp Test ($\overline{LT}$) and Blanking ($\overline{BI}$) inputs used respectively to test the display, or turn off or pulse modulate the display brightness. On the MV4368 these inputs are replaced by $\overline{RBI}$ and $\overline{RBO}$, providing automatic blanking of leading or trailing zeroes in a multidigit display. An example of leading zero suppression is shown in Fig. 8(a), and trailing zero suppression in Fig. 8(b). The $\overline{RBO}$ pin can also be wired-ORed with the output of a suitable buffer to realise pulse modulation of display brightness, as shown in Fig. 7.

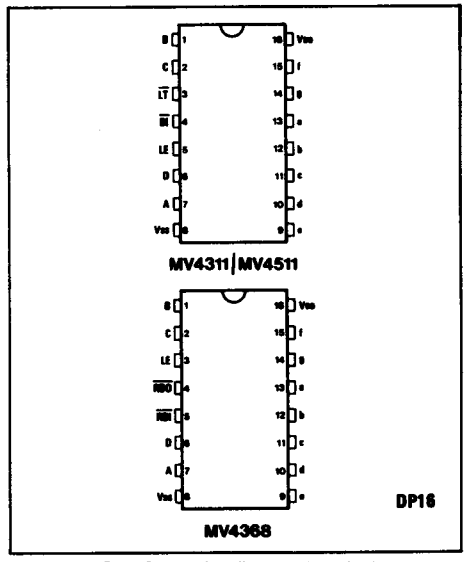


Fig.1 Connection diagrams (top view)

FEATURES

- MV4511 Compatible with 14511/4511
- MV4311 Provides 4511 Features with Hex Output
- MV4368 Second Source to TTL 9368
- Pinouts Comparable with many other Devices
- 3V to 18V Operation
- High Speed Input Latches
- Hexadecimal Decoding (MV4311/MV4368)
- Cascadable Ripple Blanking (MV4368)
- Guaranteed 20mA Output
- Supplied in 16 Pin DIL Plastic (DP) Package

PIN NAMES

A,B,C,D	Address (Data) inputs
LE	Latch Enable input
$\overline{BI}$	Blanking Input
$\overline{LT}$	Lamp Test input
$\overline{RBI}$	Ripple Blanking Input
$\overline{RBO}$	Ripple Blanking Output
a,b,c,d,e,f,g	Segment outputs
VDD	Positive supply
Vss	Ground

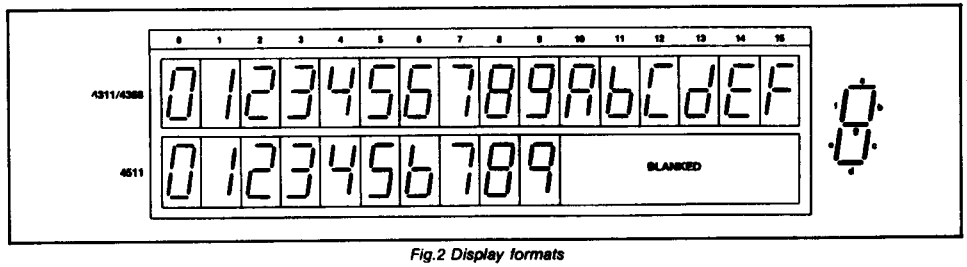


Fig.2 Display formats

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, typ. values at T_{amb} = +25°C

Characteristic	Symbol	V_{DD}(V)	Value			Unit	Conditions
			Min.	Typ.	Max.		
Input high voltage	V_{IH}	5.0	3.5	2.75		V	V_O = 1.5V or 3.5V
		10.0	7.0	5.50		V	V_O = 3.0V or 7.0V
		15.0		8.25		V	V_O = 4.5V or 10.5V
Input low voltage	V_{IL}	5.0		2.25	1.5	V	V_O = 1.5V or 3.5V
		10.0		4.50	3.0	V	V_O = 3.0V or 7.0V
		15.0		6.75		V	V_O = 4.5V or 10.5V
Input leakage current	I_{IN}				±1.0	µA	V_{IN} = Vss to V_{DD}
Output low $\overline{RBO}$	V_{OL}	5.0		0.25	0.4	V	I_{OL} = 0.4mA
		10.0			0.5	V	I_{OL} = 0.8mA
		15.0			1.5	V	I_{OL} = 2.4mA
Output high $\overline{RBO}$	V_{OH}	5.0	4.5			V	I_{OH} = -150µA
		10.0	9.5			V	I_{OH} = -350µA
		15.0	13.5			V	I_{OH} = -1100µA
Output drive voltage segment outputs	V_{OH}	5.0	4.00	4.57		V	I_{OH} = 0mA
			3.50	4.12		V	I_{OH} = -10mA
			2.80	3.75		V	I_{OH} = -20mA
		10.0	9.00	9.56		V	I_{OH} = 0mA
			8.65	9.17		V	I_{OH} = -10mA
			8.10	8.90		V	I_{OH} = -20mA
		15.0		14.59		V	I_{OH} = 0mA
				14.18		V	I_{OH} = -10mA
			13.10	13.95		V	I_{OH} = -20mA
Output drive voltage segment outputs	V_{OL}	5.0			0.4	V	I_{OL} = 0.35mA
		10.0			0.5	V	I_{OL} = 0.90mA
		15.0			1.5	V	I_{OL} = 2.4mA
Quiescent current	I_{DD}	5.0			150	µA	All inputs at Vss or V_{DD}
		10.0			300	µA	
		15.0			600	µA	

SWITCHING CHARACTERISTICS (Fig. 6)

Test conditions (unless otherwise stated):
T_{amb} = 25°C, C_L = 50pF

Characteristic	Symbol	V_{DD}(V)	Value			Unit	Conditions
			Min.	Typ.	Max.		
Output rise time	t_r	5.0		40	250	ns	
		10.0		30	160	ns	
		15.0		18		ns	
Output fall time	t_f	5.0		200		ns	
		10.0		160		ns	
		15.0		100		ns	
Data propagation delay time	t_{pLH}	5.0		640	2250	ns	
		10.0		250	900	ns	
		15.0		175			
	t_{pHL}	5.0		720	2250	ns	
		10.0		290	900	ns	
		15.0		195		ns	
Blank propagation delay time	t_{pLH}	5.0		320	1500	ns	
		10.0		130	600	ns	
		15.0		100		ns	
	t_{pHL}	5.0		485	1500	ns	
		10.0		200	600	ns	
		15.0		160		ns	
Lamp test propagation delay time	t_{pLH}	5.0		290	940	ns	
		10.0		125	375	ns	
		15.0		85		ns	
	t_{pHL}	5.0		290	940	ns	
		10.0		120	375	ns	
		15.0		90		ns	

SWITCHING CHARACTERISTICS (CONT.)

Characteristic	Symbol	V_{DD}(V)	Value			Unit	Conditions
			Min.	Typ.	Max.		
Setup time	t_{SETUP}	5.0	270	90		ns	
		10.0	114	38		ns	
		15.0		20		ns	
Hold time	t_{HOLD}	5.0	0	-90		ns	
		10.0	0	-38		ns	
		15.0		-20		ns	
Latch enable pulse width	PW_{LE}	5.0	780	260		ns	
		10.0	330	110		ns	
		15.0		65		ns	

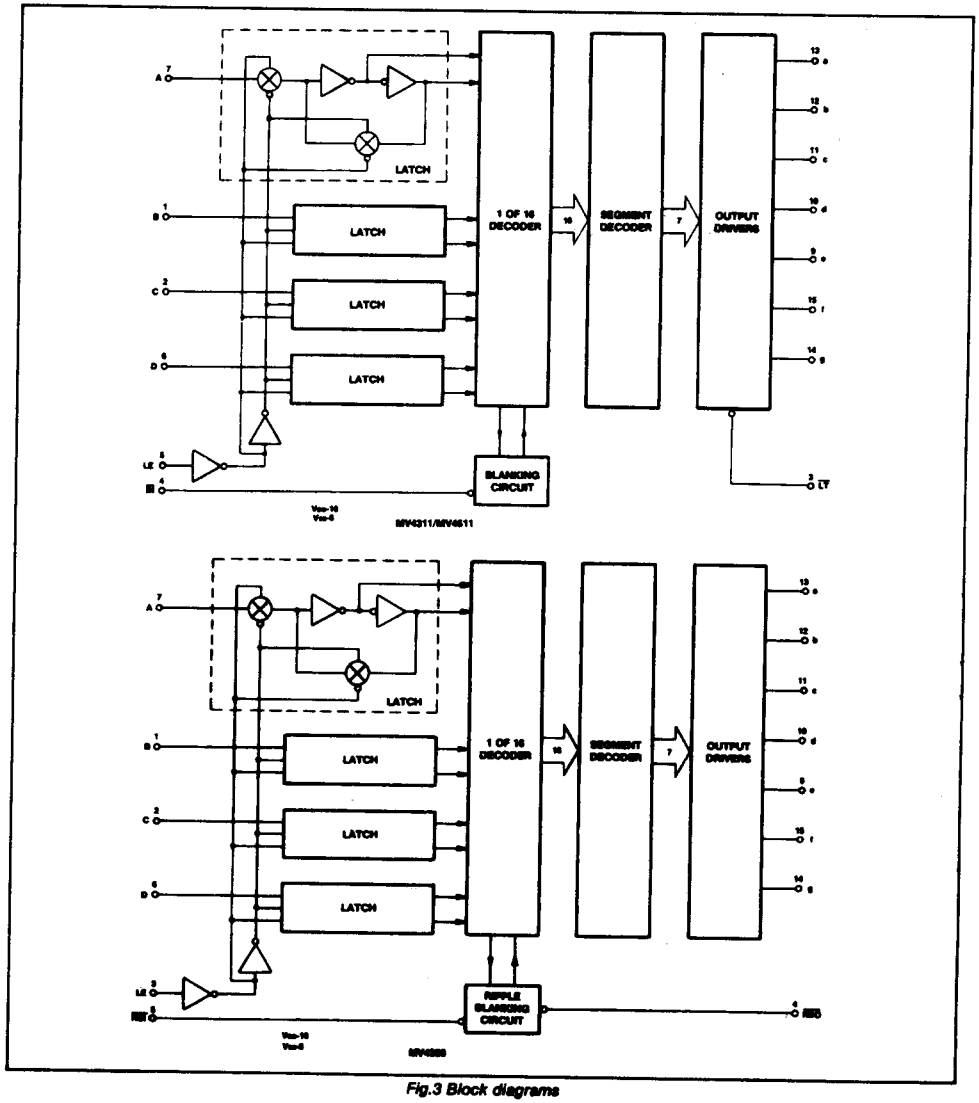
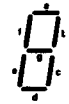


Fig.3 Block diagrams

Inputs							MV4311 Outputs							Display	MV4511 Outputs							Display
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g		a	b	c	d	e	f	g	
H	H	H	X	X	X	X	STABLE							STABLE	STABLE							STABLE
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK	L	L	L	L	L	L	L	BLANK
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8	H	H	H	H	H	H	H	8
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	H	L	H	H	H	H	H	6	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	H	L	H	H	9	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	H	H	H	L	H	H	H	A	L	L	L	L	L	L	L	BLANK
L	H	H	H	L	H	H	L	L	H	H	H	H	H	b	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	L	H	L	L	H	H	H	L	C	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	H	L	H	H	H	L	H	H	d	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	L	H	L	L	H	H	H	H	E	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	H	H	L	L	L	H	H	H	F	L	L	L	L	L	L	L	BLANK



Definition	Inputs	Outputs
H	HIGH voltage level	Sourcing current
L	LOW voltage level	Output is 'off'
X	Don't care	

Fig.4 MV4311 & MV4511 Truth tables

Inputs						MV4368 Outputs								Display
LE	$\overline{RBI}$	D	C	B	A	a	b	c	d	e	f	g	$\overline{RBO}$	
H	*	X	X	X	X	STABLE							H	STABLE
L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
L	X	L	L	L	H	L	H	H	L	L	L	L	↓	1
L	↓	L	L	H	L	H	H	L	H	H	L	H	↓	2
L	↓	L	L	H	H	H	H	H	H	L	L	H	↓	3
L	↓	L	H	L	L	L	H	H	L	L	H	H	↓	4
L	↓	L	H	L	H	H	L	H	H	L	H	H	↓	5
L	↓	L	H	H	L	H	L	H	H	H	H	H	↓	6
L	↓	L	H	H	H	H	H	H	L	L	L	L	↓	7
L	↓	H	L	L	L	H	H	H	H	H	H	H	↓	8
L	↓	H	L	L	H	H	H	H	H	L	H	H	↓	9
L	↓	H	L	H	L	H	H	H	L	H	H	H	↓	A
L	↓	H	L	H	H	L	L	H	H	H	H	H	↓	b
L	↓	H	H	L	L	H	L	L	H	H	H	L	↓	C
L	↓	H	H	L	H	L	H	H	H	H	L	H	↓	d
L	↓	H	H	H	L	H	L	L	H	H	H	H	↓	E
L	X	H	H	H	H	H	L	L	L	H	H	H	H	F
X	X	X	X	X	X	L	L	L	L	L	L	L	L**	BLANK

* $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.

** $\overline{RBO}$ used as an input overrides all other input conditions.

Definition	Inputs	Outputs
H	HIGH voltage level	Sourcing current
L	LOW voltage level	Output is 'off'
X	Don't care	

Fig.5 MV4368 Truth table

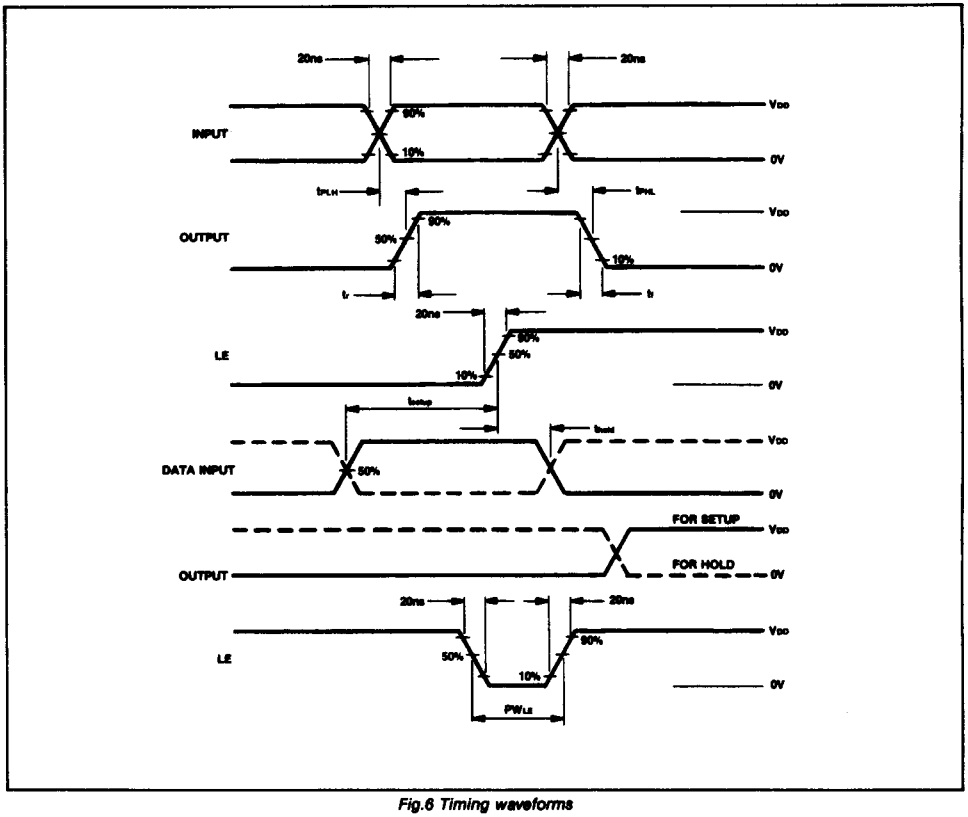


Fig.6 Timing waveforms

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded. All voltages with respect to Vss.

Parameter	Symbol	Limit	Unit
Supply voltage	V_{DD}	-0.5 to 18	V
Input voltage	V_I	-0.5 to V_{DD} +0.5	V
Maximum continuous output source current, per output	I_{OH} max.	30	mA
Maximum continuous power dissipation per output	P_{OH} max.	50	mW
Storage Temperature range	T_S	-65 to +125	°C
Operating temperature range	T_{amb}	0 to +70	°C

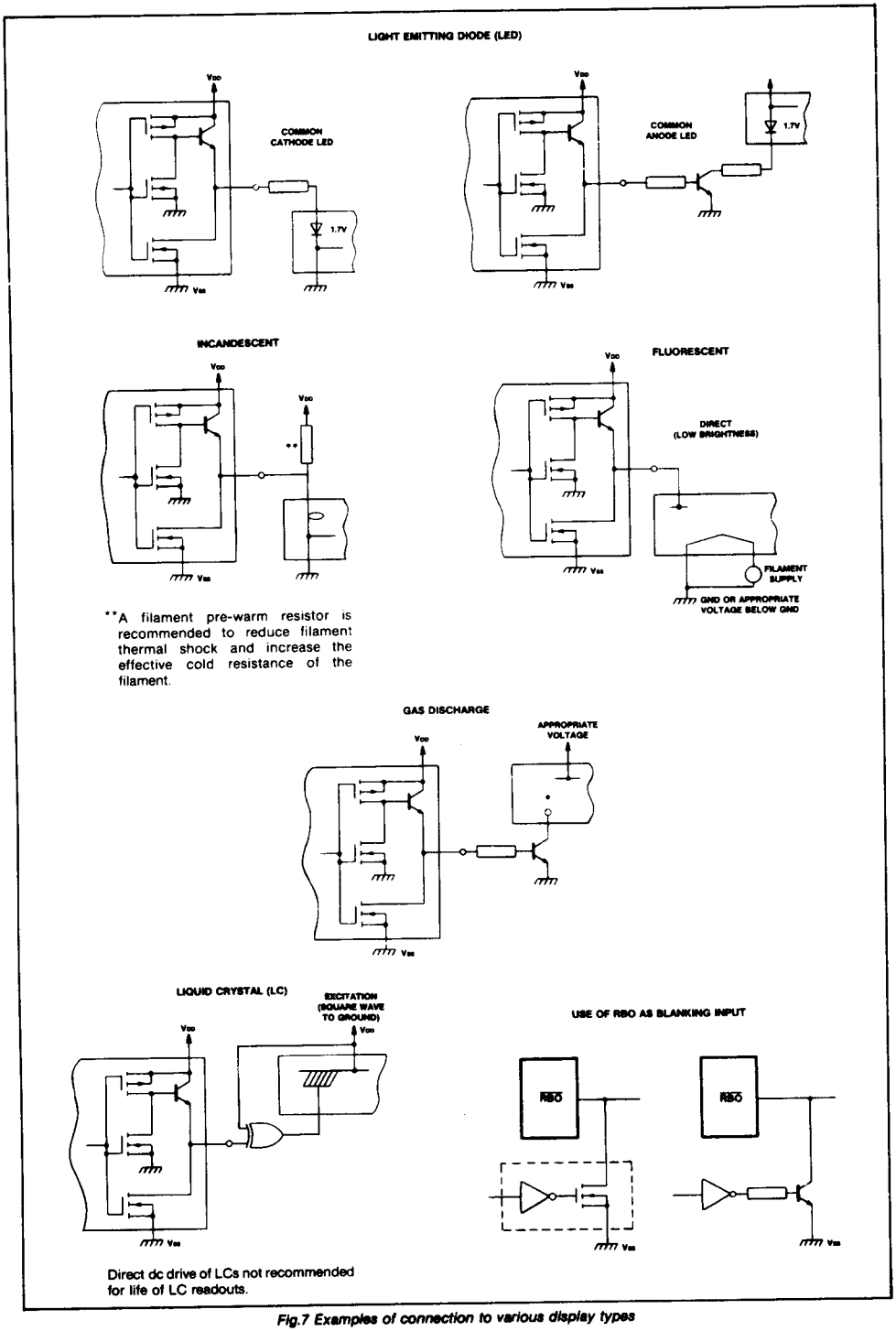


Fig.7 Examples of connection to various display types

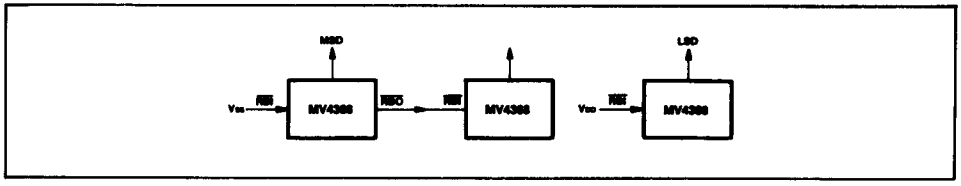


Fig.8(a) Leading zero suppression (A zero on least significant digit will not be suppressed if connected as shown)

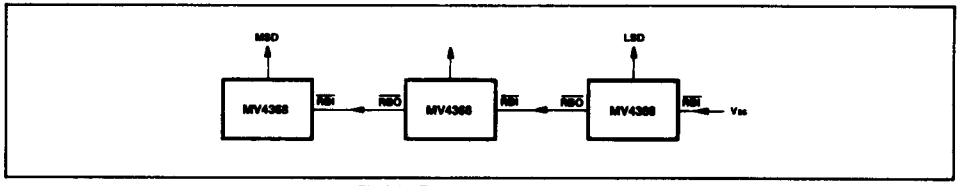


Fig.8(b) Trailing zero suppression