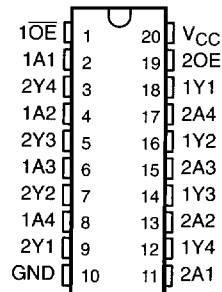


# SN54ABT241, SN74ABT241 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

D3703, JANUARY 1991 – REVISED DECEMBER 1992

- State-of-the-Art EPIC-II<sup>B</sup>™ BICMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

SN54ABT241 . . . J PACKAGE  
SN74ABT241 . . . DB, DW, OR N PACKAGE  
(TOP VIEW)



## description

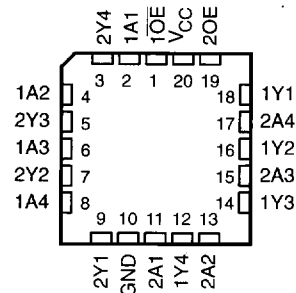
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ABT240 and 'ABT244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical  $\overline{OE}$  (active-low output-enable) inputs, and complementary OE and  $\overline{OE}$  inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT241 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT241 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT241 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT241 . . . FK PACKAGE  
(TOP VIEW)



EPIC-II<sup>B</sup> is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# SN54ABT241, SN74ABT241 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

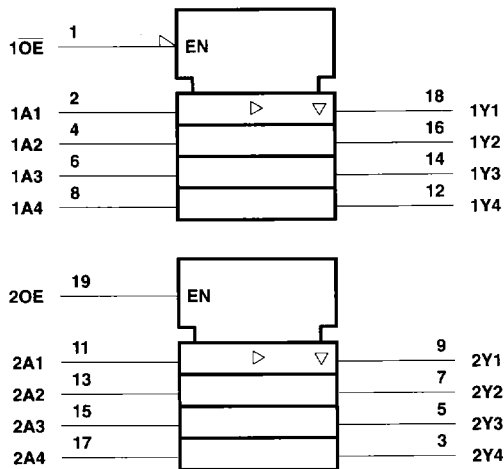
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## FUNCTION TABLES

INPUTS		OUTPUT
1OE	1A	1Y
L	H	H
L	H	H
L	L	L

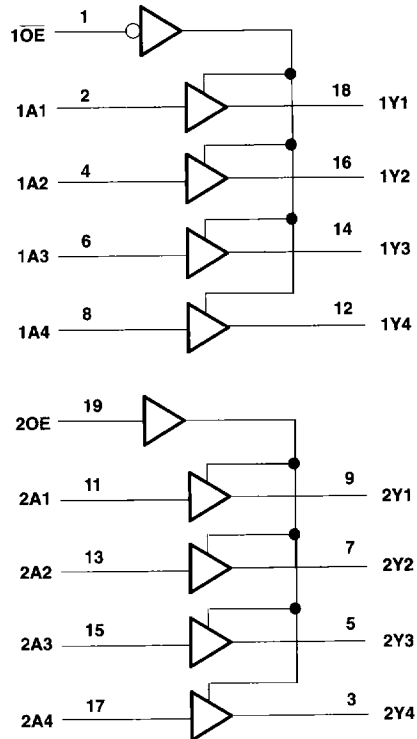
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

### logic symbol



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



**SN54ABT241, SN74ABT241**  
**OCTAL BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

D3703, JANUARY 1991 – REVISED DECEMBER 1992

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT241 .....	96 mA
SN74ABT241 .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package .....	0.65 W
DW package .....	0.85 W
N package .....	1.3 W
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

**recommended operating conditions (see Note 2)**

		SN54ABT241		SN74ABT241		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

**SN54ABT241, SN74ABT241**  
**OCTAL BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

D3703, JANUARY 1991 – REVISED DECEMBER 1992

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		T <sub>A</sub> = 25°C			SN54ABT241		SN74ABT241		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2				-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA	2.5			2.5			2.5	V
	V <sub>CC</sub> = 5 V,	I <sub>OH</sub> = -3 mA	3			3			3	
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -24 mA	2			2				
	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -32 mA	2‡						2	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA			0.55				0.55	V
	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 64 mA			0.55‡				0.55	
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = V <sub>CC</sub> or GND			±1				±1	µA
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			50				50	µA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V			-50				-50	µA
I <sub>off</sub>	V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	µA
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V	Outputs high		50				50	µA
I <sub>O<sup>§</sup></sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0,	Outputs high		1	250			250	µA
			Outputs low		24	30			30	mA
			Outputs disabled		0.5	250			250	µA
ΔI <sub>CC</sub> ¶	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Data inputs	Outputs enabled		1.5				1.5	mA
			Outputs disabled		0.05				0.05	
		Control inputs				1.5				
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V				3					pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V				8					pF

† All typical values are at V<sub>CC</sub> = 5 V.

‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

**SN54ABT241, SN74ABT241  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

D3703, JANUARY 1991 – REVISED DECEMBER 1992

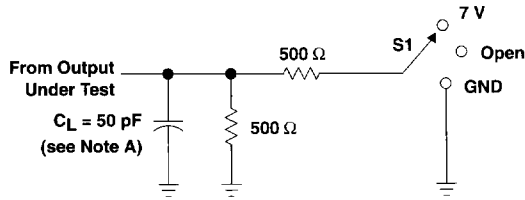
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT241		SN74ABT241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1	2.6	4.1	0.8	5.3	1	4.6	ns
$t_{PHL}$			1	2.9	4.2	0.8	5	1	4.6	
$t_{PZH}$	$\overline{OE}$ or OE	Y	1.1	4.8	6.3	1	7	1.1	6.8	ns
$t_{PZL}$			1.3	4.3	5.8	1	7	1.3	6.8	
$t_{PHZ}$	$\overline{OE}$ or OE	Y	1.6	4.6	6.1	0.8	7.9	1.6	7.1	ns
$t_{PLZ}$			1	3.9	5.4	0.8	6.2	1	5.9	

**SN54ABT241, SN74ABT241  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

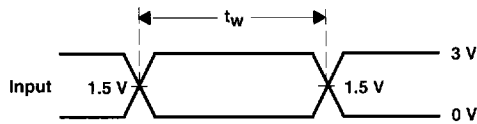
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**PARAMETER MEASUREMENT INFORMATION**

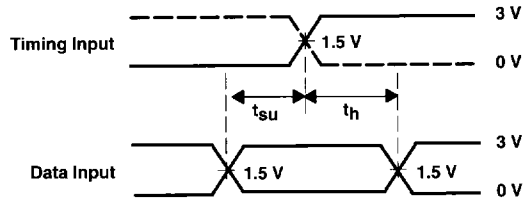


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

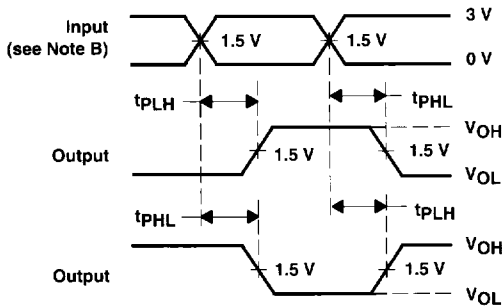
**LOAD CIRCUIT FOR OUTPUTS**



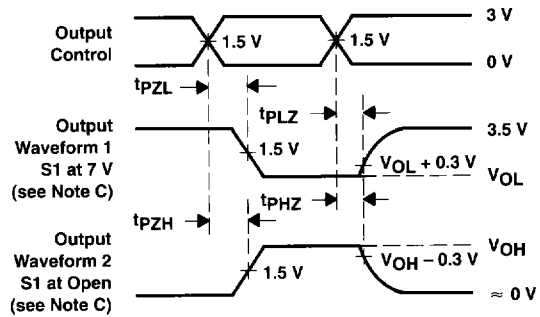
**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**