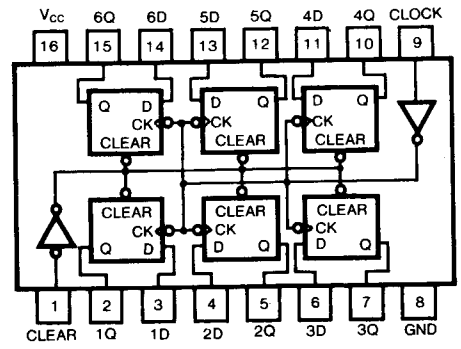
GD54/74S174

HEX D-TYPE FLIP FLOPS SINGLE RAIL OUTPUTS, COMMON DIRECT CLEAR

Feature

- Contains Six Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Application Include: Buffer/Storage Registers
  Shift Registers
  Pattern Generators

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

These monolitic, positive-edge triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positivegoing edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL or DTL circuits.

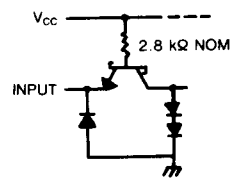
Function Table (each flip-flop)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_O	$\overline{Q}_O$

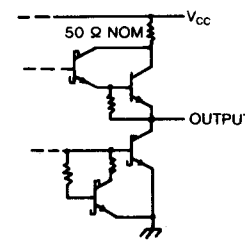
*↑=transition from low to high level.
*Q_O=the level of before the indicated steady state input conditions were established.
X=irrelevant
L=low level (steady state)
H=high level (steady state)

Schematics of Inputs and Outputs

EQUIVALENT OF ALL INPUTS



TYPICAL OF ALL OUTPUTS



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 5.5V
- Operating free-air temperature range 54S ..... −55°C to 125°C
  74S ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current					−1	mA
I_{OL}	Low-level output current					20	mA
f_{clock}	Clock frequency			0		75	MHz
t_w	Pulse width	Clock		7			ns
		Clear		10			
t_{su}	Set up time	Data input		5			ns
		Clear inactive-state		5			
t_h	Data hold time			3			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage		54			0.8	V
			74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=Min V_{IL}=Max I_{OH}=Max V_{IH}=Min	54	2.5	3.4		V
			74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max I_{OL}=Max V_{IH}=Min				0.5	V
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=5.5V				1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V				50	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.5V				−2	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)		−40		−100	mA
I_{CC}	Supply	V_{CC}=Max			90	144	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L=15pF R_L=2kΩ	75	110		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			13	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			11.5	17	ns

#For load circuit and voltage waveforms, see page 3-12.

Function Block Diagram