National Semiconductor

54ABT/74ABT543C
Octal Registered Transceiver with TRI-STATE® Outputs

General Description

The 'ABT543C octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

Features

- Back-to-back registers for storage
- Bidirectional data path
- A and B outputs have current sourcing capability of 32 mA and current sinking capability of 64 mA
- Separate controls for data flow in each direction
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

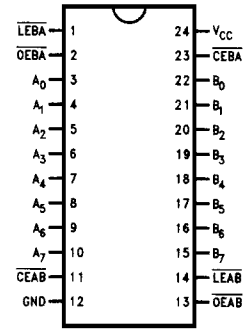
Ordering Code: See Section 10

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs
$\overline{LEAB}$, $\overline{LEBA}$	Latch Enable Inputs
$\overline{CEAB}$, $\overline{CEBA}$	Chip Enable Inputs
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Connection Diagrams

Pin Assignment for DIP, SOIC, SSOP and Flatpak



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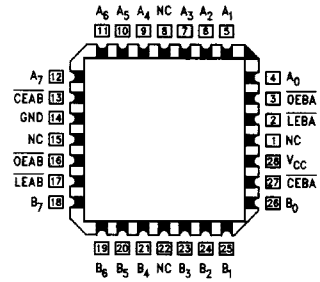
Pin Assignment for LCC



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Functional Description

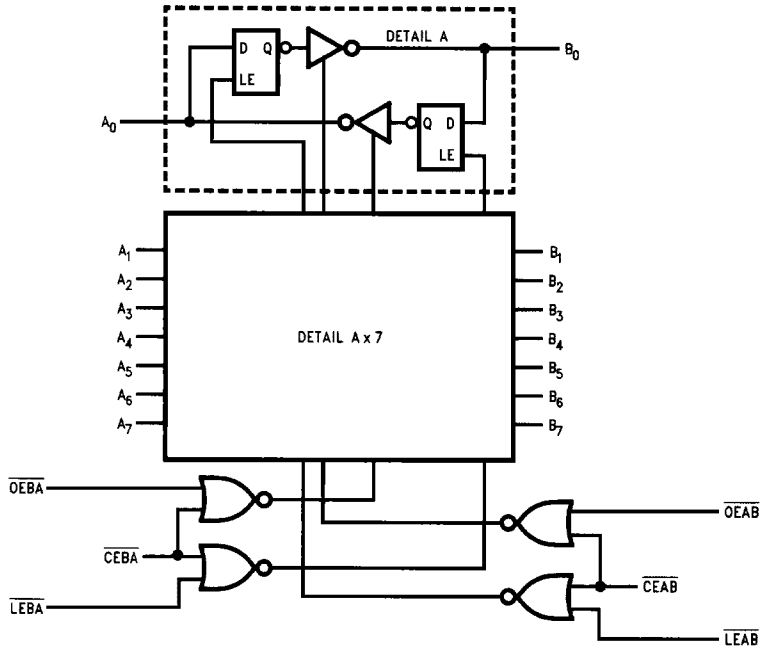
The 'ABT543C contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be low in order to enter data from the A port or take data from the B port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ low, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent low to high transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT543C			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage 54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA, (A_n, B_n)
	54ABT	2.0					I_{OH} = −24 mA, (A_n, B_n)
	74ABT	2.0					I_{OH} = −32 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage 54ABT			0.55	V	Min	I_{OL} = 48 mA, (A_n, B_n)
	74ABT			0.55			I_{OL} = 64 mA, (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 3) V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−5	μA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 3) V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			50	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I_{IL} + I_{OZL}	Output Leakage Current			−50	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			50	μA	Max	Outputs TRI-STATE All Others at V_{CC} or GND

Note 3: Guaranteed but not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT543C			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	$V_I = V_{CC} - 2.1V$ All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 2)			0.18	mA/MHz	Max	Outputs Open, $\overline{CEAB}$ and $\overline{OEAB}$ = GND, $\overline{CEBA}$ = V_{CC}, One Bit Toggling, 50% Duty Cycle, (Note 1)

Note 1: For 8-bit toggling. $I_{CCD} < 1.4$ mA/MHz.
Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC Package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.7	1.0	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.8		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25° (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.7	0.9	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.
Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.
Note 3: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SOIC and SSOP Packages): See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C V_{CC} = +5.0V C_L = 50 pF			54ABT T_A = −55°C to +125°C V_{CC} = 4.5V–5.5V C_L = 50 pF		74ABT T_A = −40°C to +85°C V_{CC} = 4.5V–5.5V C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.5	3.1	4.8			1.5	4.8	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n	1.5	3.4	5.3			1.5	5.3	ns	2-3, 5
t_{PZH} t_{PZL}	Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.5	3.6	5.8			1.5	5.8	ns	2-4
t_{PHZ} t_{PLZ}	Disable Time $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.5	4.0	6.5			1.5	6.5	ns	2-4

AC Operating Requirements (SOIC and SSOP Packages): See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C V_{CC} = +5.0V C_L = 50 pF		54ABT T_A = −55°C to +125°C V_{CC} = 4.5V–5.5V C_L = 50 pF		74ABT T_A = −40°C to +85°C V_{CC} = 4.5V–5.5V C_L = 50 pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_S(H) t_S(L)	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	1.5 1.5				1.5 1.5		ns	2-6
t_H(H) t_H(L)	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	2.0 2.0				2.0 2.0		ns	2-6
t_W(L)	Pulse Width, LOW	3.0				3.0		ns	2-3

Extended AC Electrical Characteristics (SOIC Package): See Section 2

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)			74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 5)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{toggle}	Max Toggle Frequency		100						MHz	
t_{PLH}	Progagation Delay	1.5		6.2	2.0	7.5	2.5	10.0	ns	2-3, 5
t_{PHL}	A_n to B_n or B_n to A_n	1.5		6.2	2.0	7.5	2.5	10.0		
t_{PLH}	Progagation Delay	1.5		6.5	2.0	8.0	2.5	10.5	ns	2-3, 5
t_{PHL}	$\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n	1.5		6.5	2.0	8.0	2.5	10.5		
t_{PZH}	Output Enable Time									
t_{PZL}	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.5		7.5	2.0	8.5	2.5	11.0	ns	2-4
	$\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.5		7.5	2.0	8.5	2.5	11.0		
t_{PHZ}	Output Disable Time									
t_{PLZ}	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.5		8.5	(Note 7)		(Note 7)		ns	2-4
	$\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.5		8.5						

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet

Skew (SOIC Package): See Section 2

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.0	2.0	ns	2-13
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.3	2.0	ns	2-13
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	4.0	ns	2-14
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	4.0	ns	2-17
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.5	4.5	ns	2-20

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions: $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$ (non I/O pins)
$C_{I/O}$ (Note 1)	Output Capacitance	11.0	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency, f = 1 MHz, PER MLT-STD-883B, METHOD 3012.