

## INVERTER CIRCUITS

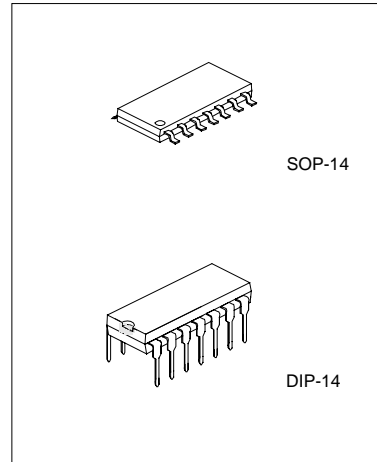
### DESCRIPTION

The UTC CD4069 consists of six inverter circuits and is manufactured using complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity, and symmetric controlled rise and fall times.

All inputs are protected from damage due to static discharge by diode clamps to VDD and VSS.

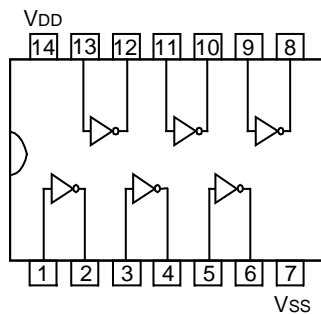
### FEATURES

- \* Wide supply voltage range: 3.0V ~ 15V.
- \* High noise immunity: 0.45 V<sub>DD</sub> typ.
- \* Low Power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS.

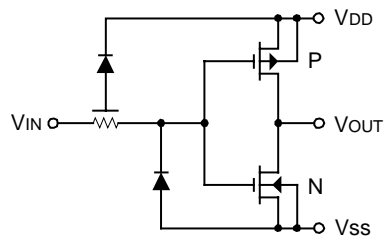


\*Pb-free plating product number: CD4069L

## PIN CONFIGURATION



## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS (Note 1, Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage	V <sub>DD</sub>	-0.5 ~ +18	V
Input Voltage	V <sub>IN</sub>	-0.5 ~ V <sub>DD</sub> +0.5	V
Storage Temperature Range	T <sub>s</sub>	-65 ~ +150	
Power Dissipation	P <sub>d</sub>	700 500	mW
	DIP-14 SOP-14		
Lead Temperature (Soldering, 10 seconds)	T <sub>L</sub>	260	

## RECOMMENDED OPERATING CONDITIONS (Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage	V <sub>DD</sub>	3 ~ 15	V
Input Voltage	V <sub>IN</sub>	0 ~ V <sub>DD</sub>	V
Operating Temperature Range	T <sub>a</sub>	-40 ~ 85	

## DC ELECTRICAL CHARACTERISTICS (Note 2, T<sub>a</sub>=25 °C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Device Current	I <sub>DD</sub>	V <sub>DD</sub> =5V, V <sub>IN</sub> =V <sub>DD</sub> or V <sub>SS</sub>			1.0	μA
		V <sub>DD</sub> =10V, V <sub>IN</sub> =V <sub>DD</sub> or V <sub>SS</sub>			2.0	
		V <sub>DD</sub> =15V, V <sub>IN</sub> =V <sub>DD</sub> or V <sub>SS</sub>			4.0	
Low Level Output Voltage	V <sub>OL</sub>	I <sub>O</sub>   < 1 μA				V
		V <sub>DD</sub> =5V		0	0.05	
		V <sub>DD</sub> =10V		0	0.05	
		V <sub>DD</sub> =15V		0	0.05	
High Level Output Voltage	V <sub>OH</sub>	I <sub>O</sub>   < 1 μA				V
		V <sub>DD</sub> =5V	4.95			
		V <sub>DD</sub> =10V	9.95			
		V <sub>DD</sub> =15V	14.95			
Low Level Input Voltage	V <sub>IL</sub>	I <sub>O</sub>   < 1 μA				V
		V <sub>DD</sub> =5V, V <sub>O</sub> =4.5V			1.0	
		V <sub>DD</sub> =10V, V <sub>O</sub> =9V			2.0	
		V <sub>DD</sub> =15V, V <sub>O</sub> =13.5V			3.0	
High Level Input Voltage	V <sub>IH</sub>	I <sub>O</sub>   < 1 μA				V
		V <sub>DD</sub> =5V, V <sub>O</sub> =0.5V	4.0			
		V <sub>DD</sub> =10V, V <sub>O</sub> =1V	8.0			
		V <sub>DD</sub> =15V, V <sub>O</sub> =1.5V	12.0			
Low Level Output Current (Note 3)	I <sub>OL</sub>	V <sub>DD</sub> =5V, V <sub>O</sub> =0.4V	0.44	0.88		mA
		V <sub>DD</sub> =10V, V <sub>O</sub> =0.5V	1.1	2.25		
		V <sub>DD</sub> =15V, V <sub>O</sub> =1.5V	3.0	8.8		
High Level Output Current (Note 3)	I <sub>OH</sub>	V <sub>DD</sub> =5V, V <sub>O</sub> =4.6V	-0.44	-0.88		mA
		V <sub>DD</sub> =10V, V <sub>O</sub> =9.5V	-1.1	-2.25		
		V <sub>DD</sub> =15V, V <sub>O</sub> =13.5V	-3.0	-8.8		
Input Current	I <sub>IN</sub>	V <sub>DD</sub> =15V, V <sub>IN</sub> =0V		-10 <sup>-5</sup>	-0.30	μA
		V <sub>DD</sub> =15V, V <sub>IN</sub> =15V		10 <sup>-5</sup>	0.30	

## AC ELECTRICAL CHARACTERISTICS\*

( $T_a=25^\circ\text{C}$ ,  $C_L=50\text{pF}$ ,  $R_L=200\text{k}\Omega$ ,  $t_r$  and  $t_f$  20 ns, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time from Input to Output	$t_{PHL}$ or $t_{PLH}$	$V_{DD}=5\text{V}$		50	90	ns
		$V_{DD}=10\text{V}$		30	60	
		$V_{DD}=15\text{V}$		25	50	
Transition Time	$t_{THL}$ or $t_{TLH}$	$V_{DD}=5\text{V}$		80	150	ns
		$V_{DD}=10\text{V}$		50	100	
		$V_{DD}=15\text{V}$		40	80	
Average Input Capacitance	$C_{IN}$	Any Gate		6	15	pF
Power Dissipation Capacitance	$C_{PD}$	Any Gate (Note 4)		12		pF

\*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed.

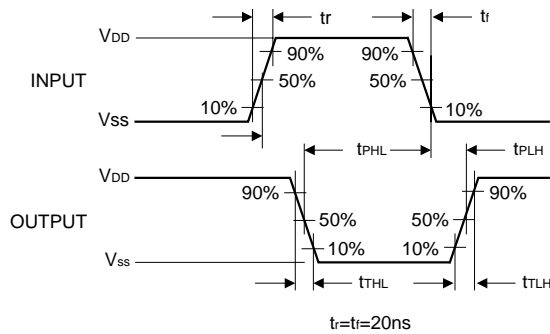
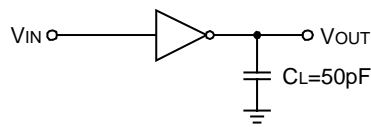
They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2:  $V_{SS}=0\text{V}$  unless otherwise specified.

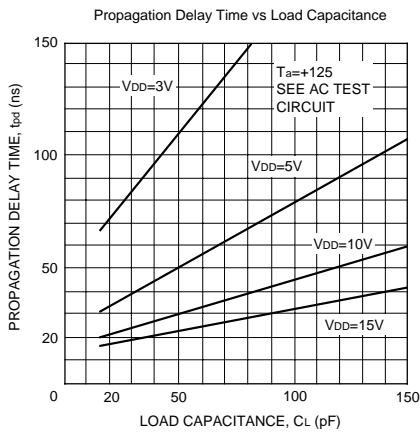
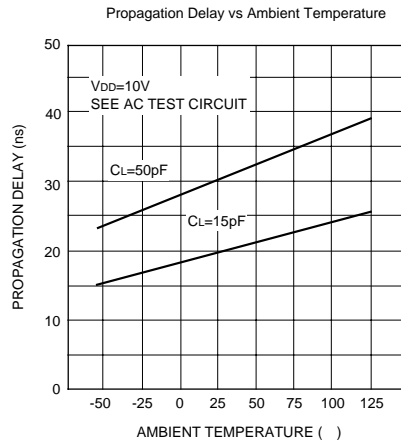
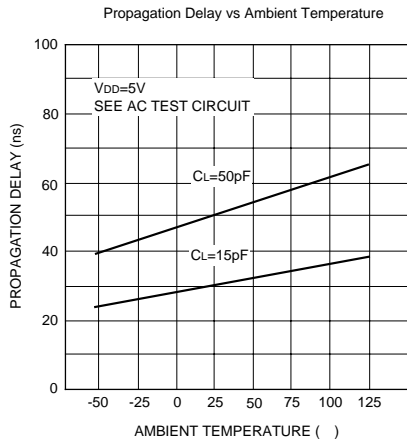
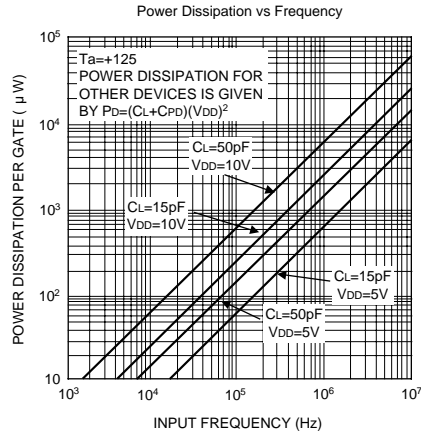
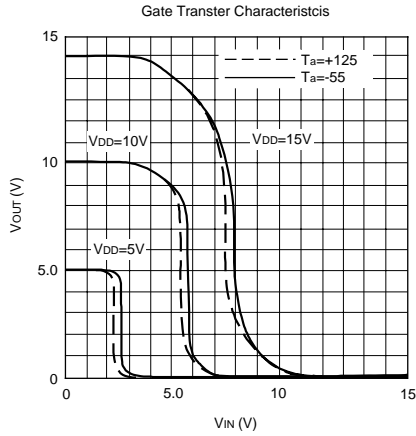
Note 3:  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

Note 4:  $C_{PD}$  determines the no load AC power consumption of any CMOS device.

## AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS



TYPICAL PERFORMANCE CHARACTERISTICS



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