Integrated Device Technology, Inc.

FAST CMOS 16-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16952AT/BT/CT/DT
IDT54/74FCT162952AT/BT/CT/DT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
  - Speed grades same as FCT-T Octals
- **Features for FCT16952AT/BT/CT/DT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162952AT/BT/CT/DT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

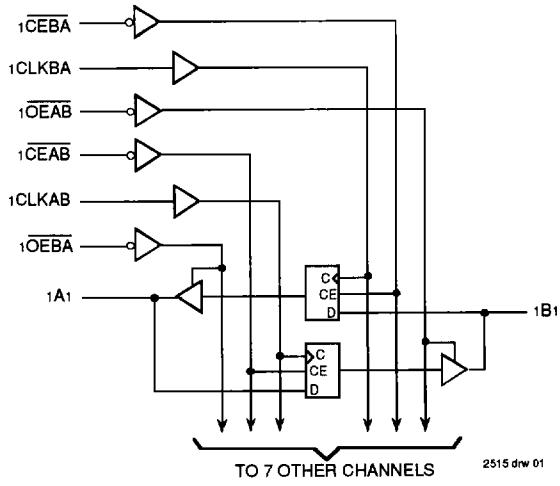
DESCRIPTION:

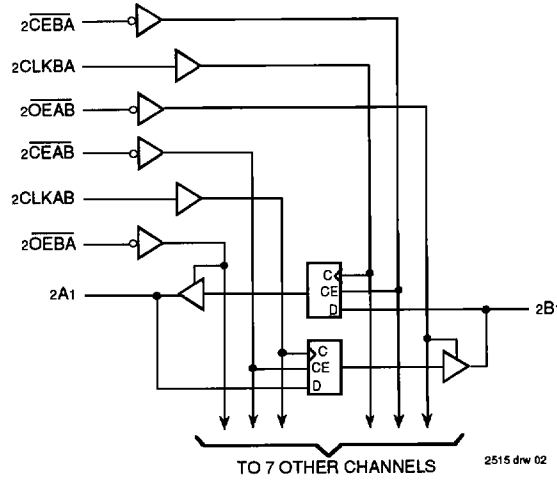
The IDT54/74FCT16952AT/BT/CT/DT and IDT54/74FCT162952AT/BT/CT/DT 16-bit registered transceivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type registered transceivers with separate input and output control for each set to permit independent control of data flow in either direction. For example, the A-to-B Enable ($x\overline{CEAB}$) must be LOW in order to enter data from the A port. xCLKAB controls the clocking function. When xCLKAB toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register. $x\overline{OEAB}$ performs the output enable function on the B port. Data flow from B port to A port is similar but requires using $x\overline{CEBA}$, xCLKBA, and $x\overline{OEBA}$ inputs. The flow-through organization of signal pins facilitates ease of layout. Full 16-bit operation can be achieved by tying the control pins of the independent transceivers together. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16952AT/BT/CT/DT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162952AT/BT/CT/DT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162952AT/BT/CT/DT are plug-in replacements for the IDT54/74FCT16952AT/BT/CT/DT and 54/74ABT16952 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM





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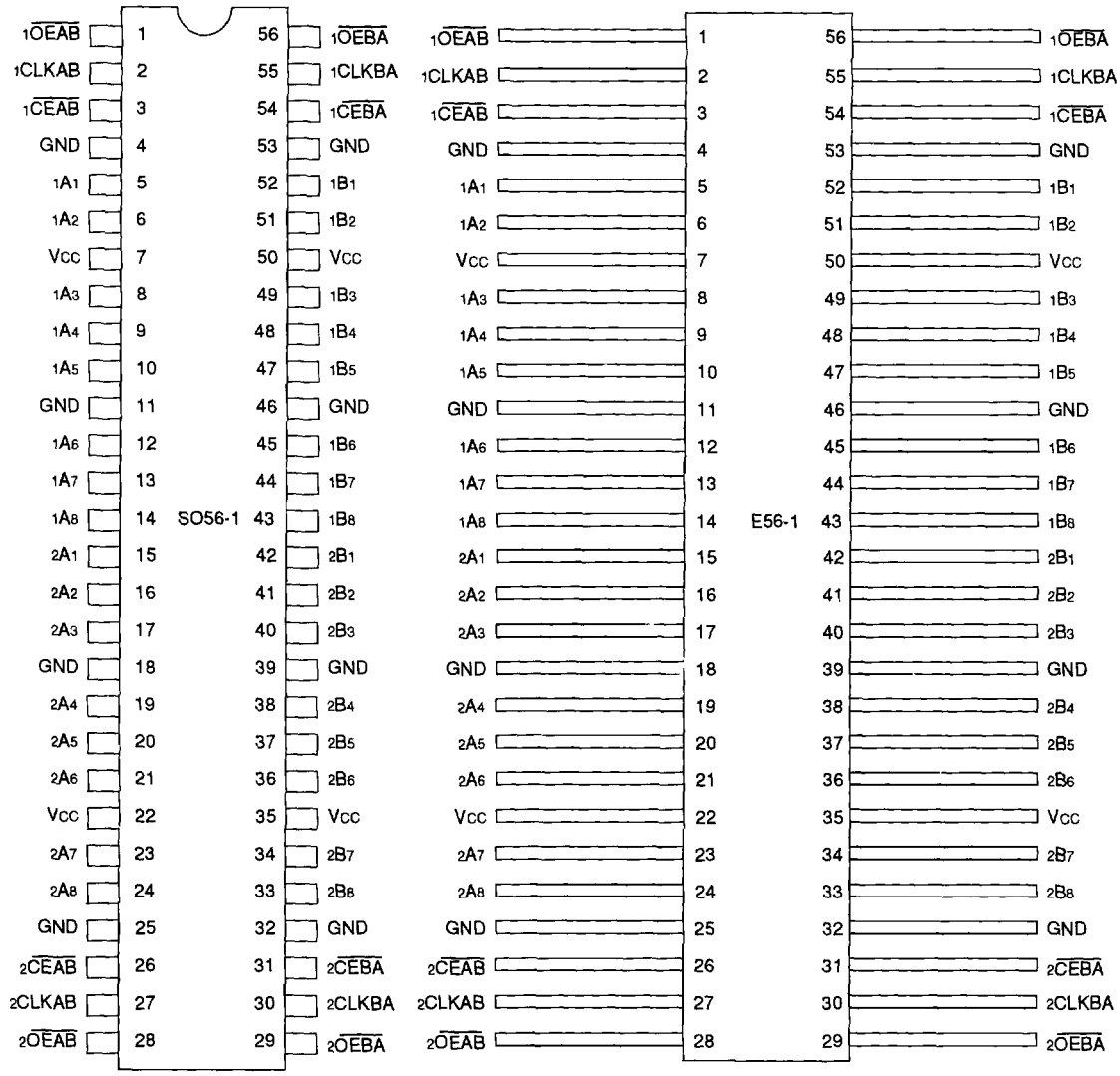
PIN CONFIGURATIONS



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PIN DESCRIPTION

Pin Names	Description
x$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
x$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
x$\overline{CEAB}$	A-to-B Clock Enable Input (Active LOW)
x$\overline{CEBA}$	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

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FUNCTION TABLE[1,3]

Inputs				Outputs
x$\overline{CEAB}$	xCLKAB	x$\overline{OEAB}$	xAx	xBx
H	X	L	X	B[2]
X	L	L	X	B[2]
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

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NOTES:
1. A-to-B data flow is shown: B-to-A data flow is similar but uses, x$\overline{CEBA}$, xCLKBA, and x$\overline{OEBA}$.
2. Level of B before the indicated steady-state input conditions were established.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT16952T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT162952T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $x\overline{OEAB}$ or $x\overline{OEBA}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	2.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	4.2	
		V_{CC} = Max., Outputs Open f_{CP}= 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} Sixteen Bits Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.3	21[5]	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16952AT/162952AT				FCT16952BT/162952BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	ns
tPZH tPZL	Output Enable Time $x\overline{OEBA}$, $x\overline{OEAB}$ to xAx, xBx		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
tPHZ tPLZ	Output Disable Time $x\overline{OEBA}$, $x\overline{OEAB}$ to xAx, xBx		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	ns
tSU	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.0	—	2.0	—	1.5	—	1.5	—	ns
tSU	Set-up Time, HIGH or LOW $x\overline{CEAB}$, $x\overline{CEBA}$ to xCLKAB, xCLKBA		3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $x\overline{CEAB}$, $x\overline{CEBA}$ to xCLKAB, xCLKBA		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	Pulse Width HIGH or LOW xCLKAB or xCLKBA[3]		3.0	—	3.0	—	3.0	—	3.0	—	ns
tSK(o)	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	ns

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Symbol	Parameter	Condition[1]	FCT16952CT/162952CT				FCT16952DT/162952DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	CL = 50pF RL = 500Ω	2.0	6.3	2.0	7.3	2.0	4.5	—	—	ns
tPZH tPZL	Output Enable Time $x\overline{OEBA}$, $x\overline{OEAB}$ to xAx, xBx		1.5	7.0	1.5	8.0	1.5	5.6	—	—	ns
tPHZ tPLZ	Output Disable Time $x\overline{OEBA}$, $x\overline{OEAB}$ to xAx, xBx		1.5	6.5	1.5	7.5	1.5	4.3	—	—	ns
tSU	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	1.5	—	—	—	ns
tH	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		1.5	—	1.5	—	1.0	—	—	—	ns
tSU	Set-up Time, HIGH or LOW $x\overline{CEAB}$, $x\overline{CEBA}$ to xCLKAB, xCLKBA		3.0	—	3.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW $x\overline{CEAB}$, $x\overline{CEBA}$ to xCLKAB, xCLKBA		2.0	—	2.0	—	1.0	—	—	—	ns
tW	Pulse Width HIGH or LOW xCLKAB or xCLKBA[3]		3.0	—	3.0	—	3.0	—	—	—	ns
tSK(o)	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	—	ns

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NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

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