# CMOS 16-BIT LEVEL SHIFTING BUS TRANSCEIVER WITH 3-STATE OUTPUTS

**IDT74AUC164245**

## FEATURES:

- **$V_{DDA}$ AND $V_{DDB}$ = 0.8V - 2.7V**
- **Inputs/outputs tolerant up to 3.6V**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **Supports Hot insertion:**
- **A and B port output drivers: ±9mA @ 2.3V**
- **Available in TSSOP, TVSOP, and VFBGA packages**

## APPLICATIONS:

- **High performance, low voltage communications systems**
- **High performance, low voltage computing systems**

## DESCRIPTION:

This 16-bit level shifting bus transceiver is built using advanced CMOS technology. The AUC164245 is ideal for asynchronous communications between data buses. The control function implementation minimizes external timing requirements.

The AUC164245 16-bit level shifting bus transceiver contains two separate supply rails. The B port is designed to track $V_{DDB}$, which accepts voltages from 0.8V to 2.7V. The A port and control inputs are designed to track $V_{DDA}$, which accepts voltages from 0.8V to 2.7V. This allows for user-selectable translation for various level shifting system environments.

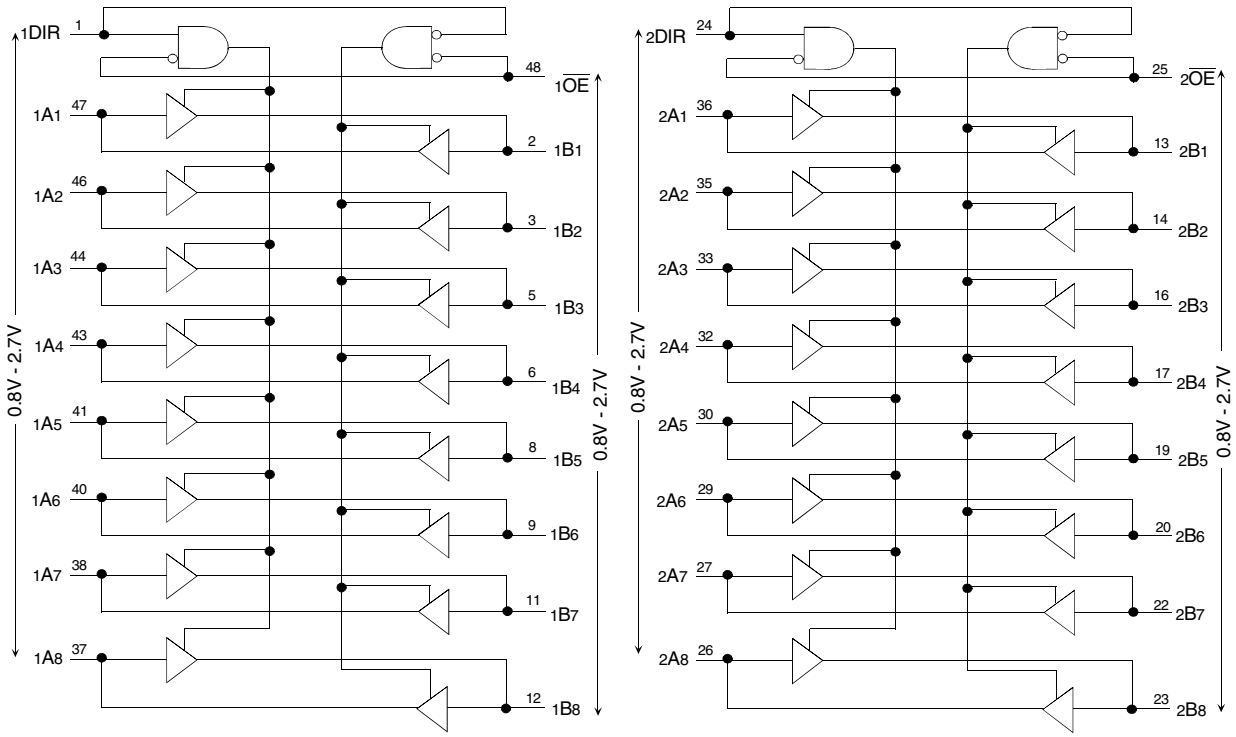
This device can be used as one 16-bit transceiver or two 8-bit transceivers. It allows data transmission from A bus to B bus or from B bus to A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

This device is fully specified for partial power-down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The AUC164245 A and B ports are designed with ±9mA output drivers. These drivers are capable of driving moderate loads while maintaining high speed performance.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{DDA}$ through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## FUNCTIONAL BLOCK DIAGRAM



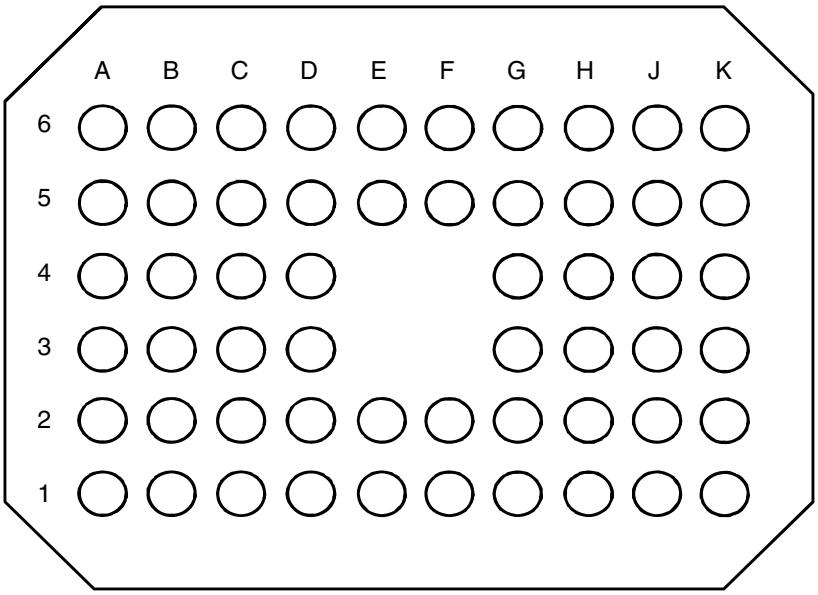
## PINOUT CONFIGURATION

| | A | B | C | D | E | F | G | H | J | K |
|---|---|---|---|---|---|---|---|---|---|---|
| 6 | $1\overline{OE}$ | 1A2 | 1A4 | 1A6 | 1A8 | 2A1 | 2A3 | 2A5 | 2A7 | $2\overline{OE}$ |
| 5 | NC | 1A1 | 1A3 | 1A5 | 1A7 | 2A2 | 2A4 | 2A6 | 2A8 | NC |
| 4 | NC | GND | $V_{DDA}$ | GND | | | GND | $V_{DDA}$ | GND | NC |
| 3 | NC | GND | $V_{DDB}$ | GND | | | GND | $V_{DDB}$ | GND | NC |
| 2 | NC | 1B1 | 1B3 | 1B5 | 1B7 | 2B2 | 2B4 | 2B6 | 2B8 | NC |
| 1 | 1DIR | 1B2 | 1B4 | 1B6 | 1B8 | 2B1 | 2B3 | 2B5 | 2B7 | 2DIR |

**NOTE:**
NC = No Internal Connection

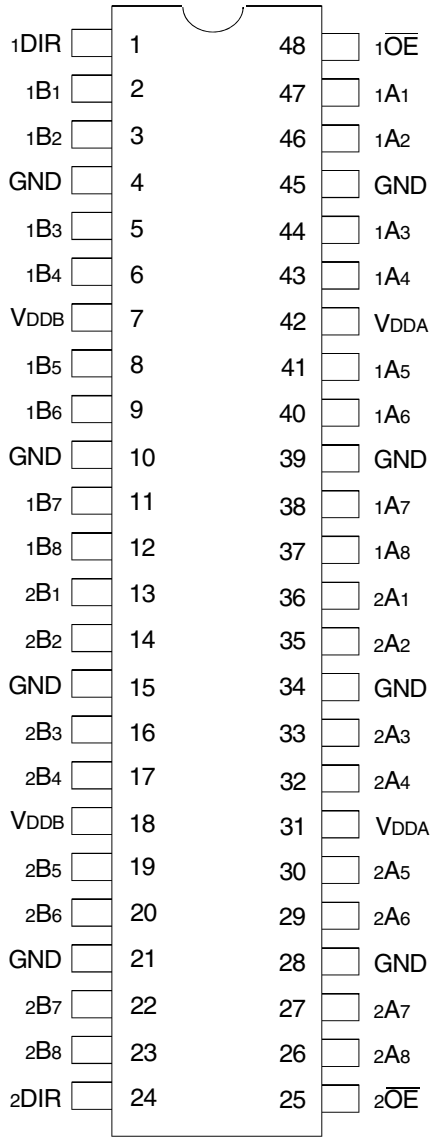
**VFBGA**

## 56 BALL VFBGA PACKAGE LAYOUT




**TOP VIEW**

## PIN CONFIGURATION




**TSSOP/ TVSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS FOR $V_{DDA}$ OR $V_{DDB}$(1)

| Symbol | Description | | Max | Unit |
|---|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND (all input and $V_{DD}$ terminals) | | –0.5 to +3.6 | V |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (any I/O or Output terminals in high-impedance or power-off state) | | –0.5 to +3.6 | V |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (any I/O or Output terminals in high or low state) | | –0.5 to +3.6 | V |
| $T_{STG}$ | Storage Temperature | | –65 to +150 | ° C |
| $I_{OUT}$ | Continuous DC Output Current | | ±20 | mA |
| $I_{IK}$ | Continuous Clamp Current | $V_I > V_{DD}$ | +50 | mA |
| | | $V_I < 0$ | –50 | |
| $I_{OK}$ | Continuous Clamp Current, $V_O < 0$ | | –50 | mA |
| $I_{DD}$ $I_{SS}$ | Continuous Current through each $V_{DD}$ or GND | | ±100 | mA |

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz, $V_{DDA}$ or $V_{DDB}$ = 2.5V)

| Symbol | Parameter | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance(1) | $V_{IN}$ = $V_{DD}$ or GND | 2.5 | 4 | pF |
| $C_{I/O}$ | I/O Port Capacitance(2) | $V_{I/O}$ = $V_{DD}$ or GND | 6 | 7 | pF |

**NOTES:**
1. Applies to the Control Inputs.
2. Applies to ports A and B.

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| x$\overline{OE}$ | 3-State Output Enable Control Inputs (Active Low)(1) |
| xDIR | Direction Control Inputs(1) |
| xAx | A Side Inputs or 3-State Outputs(1) |
| xBx | B Side Inputs or 3-State Outputs(2) |
| $V_{DDA}$ | Supply for A port, x$\overline{OE}$, xDIR |
| $V_{DDB}$ | Supply for B port |

**NOTES:**
1. Powered from $V_{DDA}$.
2. Powered from $V_{DDB}$.

## FUNCTION TABLE (EACH 8-BIT SECTION)(1)

| Inputs | | |
|---|---|---|
| x$\overline{OE}$ | xDIR | Outputs |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | Z |

**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance

## RECOMMENDED OPERATING CHARACTERISTICS(1)

| Symbol(2) | Parameter | Test Conditions(2) | Min.(2) | Max.(2) | Unit |
|---|---|---|---|---|---|
| $V_{DDX}$ | Supply Voltage | | 0.8 | 2.7 | V |
| $V_{IH}$(3) | Input HIGH Voltage Level | $V_{DDX}$ = 0.8V | $V_{DDX}$ | — | V |
| | | $V_{DDX}$ = 1.1V to 1.3V | 0.65 x $V_{DDX}$ | — | |
| | | $V_{DDX}$ = 1.4V to 1.6V | 0.65 x $V_{DDX}$ | — | |
| | | $V_{DDX}$ = 1.65V to 1.95V | 0.65 x $V_{DDX}$ | — | |
| | | $V_{DDX}$ = 2.3V to 2.7V | 1.7 | — | |
| $V_{IL}$(3) | Input LOW Voltage Level | $V_{DDX}$ = 0.8V | — | 0 | V |
| | | $V_{DDX}$ = 1.1V to 1.3V | — | 0.35 x $V_{DDX}$ | |
| | | $V_{DDX}$ = 1.4V to 1.6V | — | 0.35 x $V_{DDX}$ | |
| | | $V_{DDX}$ = 1.65V to 1.95V | — | 0.35 x $V_{DDX}$ | |
| | | $V_{DDX}$ = 2.3V to 2.7V | — | 0.7 | |
| $V_I$ | Input Voltage | | 0 | 2.7 | V |
| $V_O$ | Output Voltage | Active State | 0 | $V_{DDX}$ | V |
| | | 3-State | 0 | 2.7 | |
| $I_{OH}$ | HIGH Level Output Current | $V_{DDX}$ = 0.8V | — | –0.7 | mA |
| | | $V_{DDX}$ = 1.1V | — | –3 | |
| | | $V_{DDX}$ = 1.4V | — | –5 | |
| | | $V_{DDX}$ = 1.65V | — | –8 | |
| | | $V_{DDX}$ = 2.3V | — | –9 | |
| $I_{OL}$ | LOW Level Output Current | $V_{DDX}$ = 0.8V | — | 0.7 | mA |
| | | $V_{DDX}$ = 1.1V | — | 3 | |
| | | $V_{DDX}$ = 1.4V | — | 5 | |
| | | $V_{DDX}$ = 1.65V | — | 8 | |
| | | $V_{DDX}$ = 2.3V | — | 9 | |
| $\Delta t/\Delta v$ | Input Transition Rise or Fall Time | | — | 5 | ns/V |
| $T_A$ | Operating Free-Air Temperature | | –40 | +85 | °C |

**NOTES:**

1. All unused inputs of the device must be held at $V_{DD}$ or GND to ensure proper operation.
2. Where $V_{DDX}$ refers to either $V_{DDA}$ or $V_{DDB}$, depending on which side output A or B is on.
3. $V_{IL}$,$V_{IH}$ limits apply for outputs operating at adjacent voltage ranges. For example, 1.8V $V_{IL}$/$V_{IH}$ limits apply for outputs operating at 1.5V or 2.5V.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (A PORT OR B PORT)(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Conditions: $T_A$ = –40°C to +85°C

| Symbol | Parameter | | Test Conditions(2) | | Min.(2) | Typ.(2) | Max.(2) | Unit |
|---|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH or LOW Current | Data Inputs | $V_{DDX}$ = 2.7V, $V_I$ = $V_{DDX}$ or GND | | — | — | ±10 | µA |
| $I_{IL}$ | | Control Inputs | | | — | — | ±5 | |
| $I_{OFF}$ | Input/Output Power Off Leakage | | $V_{DDX}$ = 0V, $V_{IN}$ or $V_O \leq$ 2.7V | | — | — | ±10 | µA |
| $I_{OZH}$(3) | High Impedance Output Current | | $V_{DDX}$ = 2.7V | $V_O$ = $V_{DDX}$ | — | — | ±10 | µA |
| $I_{OZL}$(3) | (3-State Output Pins) | | | $V_O$ = GND | — | — | ±10 | |
| $I_{DDL}$ | Quiescent Power Supply Current | | $V_{DDX}$ = 0.8V to 2.7V | | — | — | 20 | µA |
| $I_{DDH}$ | | | $V_{IN}$ = GND or $V_{DDX}$ | | | | | |
| $I_{DDZ}$ | | | | | | | | |

**NOTES:**
1. All unused inputs of the device must be held at $V_{DD}$ or GND to ensure proper operation.
2. Where $V_{DDX}$ refers to either $V_{DDA}$ or $V_{DDB}$, depending on which side output A or B is on.
3. For the I/O ports, the parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.

## OUTPUT DRIVE CHARACTERISTICS (A PORT OR B PORT)

| Symbol | Parameter | Test Conditions(1,6) | | Min.(6) | Typ. | Max.(6) | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{DDX}$ = 0.8V - 2.7V | $I_{OH}$ = –100µA | $V_{DDX}$ - 0.1 | — | — | V |
| | | $V_{DDX}$ = 0.8V | $I_{OH}$ = –0.7mA | — | 0.55 | — | |
| | | $V_{DDX}$ = 1.1V(2) | $I_{OH}$ = –3mA | 0.8 | — | — | |
| | | $V_{DDX}$ = 1.4V(3) | $I_{OH}$ = –5mA | 1 | — | — | |
| | | $V_{DDX}$ = 1.65V(4) | $I_{OH}$ = –8mA | 1.2 | — | — | |
| | | $V_{DDX}$ = 2.3V(5) | $I_{OL}$ = –9mA | 1.8 | — | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{DDX}$ = 0.8V - 2.7V | $I_{OL}$ = 100µA | — | — | 0.2 | V |
| | | $V_{DDX}$ = 0.8V | $I_{OL}$ = 0.7mA | — | 0.25 | — | |
| | | $V_{DDX}$ = 1.1V(2) | $I_{OL}$ = 3mA | — | — | 0.3 | |
| | | $V_{DDX}$ = 1.4V(3) | $I_{OL}$ = 5mA | — | — | 0.4 | |
| | | $V_{DDX}$ = 1.65V(4) | $I_{OL}$ = 8mA | — | — | 0.45 | |
| | | $V_{DDX}$ = 2.3V(5) | $I_{OL}$ = 9mA | — | — | 0.6 | |

**NOTES:**
1. $V_{IL}$ and $V_{IH}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS table for the appropriate $V_{DD}$ range. $T_A$ = -40°C to +85°C.
2. Demonstrates operation for nominal $V_{DDA}$ or $V_{DDB}$ = 1.2V.
3. Demonstrates operation for nominal $V_{DDA}$ or $V_{DDB}$ = 1.5V.
4. Demonstrates operation for nominal $V_{DDA}$ or $V_{DDB}$ = 1.8V.
5. Demonstrates operation for nominal $V_{DDA}$ or $V_{DDB}$ = 2.5V.
6. Where $V_{DDX}$ refers to either $V_{DDA}$ or $V_{DDB}$, depending on which side output A or B is on.

## OPERATING CHARACTERISTICS, A TO B, $V_{DDA}$ AND $V_{DDB}$ = 2.5V, $T_A$ = 25°C

| Symbol | Parameter | | Test Conditions | Typ. | Unit |
|---|---|---|---|---|---|
| $C_{PDA}$ | Power Dissipation Capacitance | Outputs Enabled | $C_L$ = 0pF | 3 | pF |
| | | Outputs Disabled | f = 10MHz | 0.4 | |
| $C_{PDB}$ | Power Dissipation Capacitance | Outputs Enabled | $C_L$ = 0pF | 1.4 | pF |
| | | Outputs Disabled | f = 10MHz | 1.5 | |

## OPERATING CHARACTERISTICS, B TO A, $V_{DDA}$ AND $V_{DDB}$ = 2.5V, $T_A$ = 25°C

| Symbol | Parameter | | Test Conditions | Typ. | Unit |
|---|---|---|---|---|---|
| $C_{PDA}$ | Power Dissipation Capacitance | Outputs Enabled | $C_L$ = 0pF | 14 | pF |
| | | Outputs Disabled | f = 10MHz | 1.5 | |
| $C_{PDB}$ | Power Dissipation Capacitance | Outputs Enabled | $C_L$ = 0pF | 3 | pF |
| | | Outputs Disabled | f = 10MHz | 0.4 | |

## SWITCHING CHARACTERISTICS, $V_{DDA}$ = 0.8[1,2]

| Symbol | Parameter | $V_{DDB}$ = 0.8V Typ. | $V_{DDB}$ = 1.2V±0.1V Typ. | Unit |
|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay[3] xAx to xBx | 10 | 5 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay[3] xBx to xAx | 10 | 11 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time[4] x$\overline{OE}$ to xAx | 7.5 | 7.5 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time[4] x$\overline{OE}$ to xAx | 8.5 | 8.5 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time x$\overline{OE}$ to xBx | 10.5 | 4.8 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time x$\overline{OE}$ to xBx | 12 | 6.8 | ns |

## SWITCHING CHARACTERISTICS, $V_{DDA}$ = 1.2V ± 0.1[1]

| Symbol | Parameter | $V_{DDB}$ = 0.8V | $V_{DDB}$ = 1.2V±0.1V | | $V_{DDB}$ = 1.5V±0.1V | | $V_{DDB}$ = 1.8V±0.15V | | | $V_{DDB}$ = 2.5V±0.2V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ. | Min. | Max. | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay[3] xAx to xBx | 11 | 1 | 4.5 | 0.5 | 3.5 | 0.5 | 2 | 3.5 | 0.5 | 3 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay[3] xBx to xAx | 5 | 1 | 4.5 | 0.5 | 4.5 | 0.5 | 3 | 4.2 | 0.5 | 4 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time[4] x$\overline{OE}$ to xAx | 3.2 | 0.7 | 4.6 | 0.7 | 4.6 | 0.7 | 3.2 | 4.6 | 0.7 | 4.6 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time[4] x$\overline{OE}$ to xAx | 4.6 | 0.8 | 6.2 | 0.8 | 6.2 | 0.8 | 4.6 | 6.2 | 0.8 | 6.2 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time x$\overline{OE}$ to xBx | 9 | 0.7 | 4.6[4] | 0.7 | 3.6 | 0.7 | 2.2 | 3.6 | 0.7 | 3.5 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time x$\overline{OE}$ to xBx | 9.5 | 0.8 | 6.2[4] | 0.8 | 5 | 0.8 | 3.5 | 4.8 | 0.8 | 4.3 | ns |

**NOTES:**
1. See TEST CIRCUITS AND WAVEFORMS. $T_A$ = -40°C to +85°C.
2. The temperature range for the 0.8V node is 0°C to +85°C.
3. Propagation delay is symmetrical A-B, depending only on input and output $V_{DD}$.
4. Enable/Disable to xAx depends on $V_{DDA}$ only. Times for xBx same if $V_{DDA}$ = $V_{DDB}$.

## SWITCHING CHARACTERISTICS, $V_{DDA}$ = 1.5V ± 0.1(1)

| Symbol | Parameter | $V_{DDB}$ = 1.2V±0.1V | | $V_{DDB}$ = 1.5V±0.1V | | $V_{DDB}$ = 1.8V±0.15V | | | $V_{DDB}$ = 2.5V±0.2V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay(2) xAx to xBx | 0.5 | 4.5 | 0.5 | 3.3 | 0.5 | 2.3 | 3.1 | 0.5 | 2.6 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay(2) xBx to xAx | 0.5 | 3.5 | 0.5 | 3.3 | 0.5 | 2 | 3 | 0.5 | 2.8 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time(3) x$\overline{OE}$ to xAx | 0.7 | 3.3 | 0.7 | 3.1 | 0.7 | 2.3 | 3.3 | 0.7 | 3.3 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time(3) x$\overline{OE}$ to xAx | 0.8 | 4.5 | 0.8 | 4.7 | 0.8 | 3 | 4.5 | 0.8 | 4.5 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time x$\overline{OE}$ to xBx | 0.7 | 4.3 | 0.7 | 3.1(3) | 0.7 | 2.3 | 3.3 | 0.7 | 3.2 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time x$\overline{OE}$ to xBx | 0.8 | 5.5 | 0.8 | 4.7(3) | 0.8 | 3 | 4.5 | 0.8 | 3.7 | ns |

## SWITCHING CHARACTERISTICS, $V_{DDA}$ = 1.8V ± 0.15(1)

| Symbol | Parameter | $V_{DDB}$ = 1.2V±0.1V | | $V_{DDB}$ = 1.5V±0.1V | | $V_{DDB}$ = 1.8V±0.15V | | | $V_{DDB}$ = 2.5V±0.2V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay(2) xAx to xBx | 0.5 | 4.2 | 0.5 | 3 | 0.5 | 2 | 2.8 | 0.5 | 2.5 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay(2) xBx to xAx | 0.5 | 3.5 | 0.5 | 3.1 | 0.5 | 2 | 2.8 | 0.5 | 2.6 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time(3) x$\overline{OE}$ to xAx | 0.7 | 3 | 0.7 | 3 | 0.7 | 2.1 | 3 | 0.7 | 3 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time(3) x$\overline{OE}$ to xAx | 0.8 | 4.3 | 0.8 | 4.3 | 0.8 | 3.2 | 4.3 | 0.8 | 4.3 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time x$\overline{OE}$ to xBx | 0.7 | 4 | 0.7 | 3 | 0.7 | 2.1(3) | 3(3) | 0.7 | 2.8 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time x$\overline{OE}$ to xBx | 0.8 | 5.3 | 0.8 | 4.3 | 0.8 | 3.2(3) | 4.3(3) | 0.8 | 3 | ns |

## SWITCHING CHARACTERISTICS, $V_{DDA}$ = 2.5V ± 0.2(1)

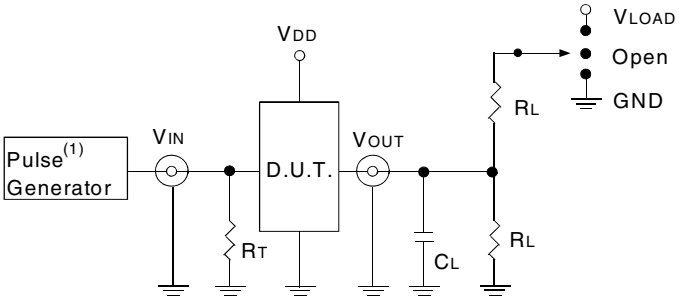
| Symbol | Parameter | $V_{DDB}$ = 1.2V±0.1V | | $V_{DDB}$ = 1.5V±0.1V | | $V_{DDB}$ = 1.8V±0.15V | | | $V_{DDB}$ = 2.5V±0.2V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Typ. | Max. | Min. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay(2) xAx to xBx | 0.5 | 4 | 0.5 | 2.8 | 0.5 | 1.8 | 2.6 | 0.5 | 2.2 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay(2) xBx to xAx | 0.5 | 3 | 0.5 | 2.6 | 0.5 | 1.7 | 2.5 | 0.5 | 2.2 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time(3) x$\overline{OE}$ to xAx | 0.7 | 2.6 | 0.7 | 2.6 | 0.7 | 1.8 | 2.6 | 0.7 | 2.6 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time(3) x$\overline{OE}$ to xAx | 0.8 | 2.9 | 0.8 | 2.9 | 0.8 | 2 | 2.9 | 0.8 | 2.9 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time x$\overline{OE}$ to xBx | 0.7 | 4 | 0.7 | 2.8 | 0.7 | 2 | 3.1 | 0.7 | 2.6(3) | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time x$\overline{OE}$ to xBx | 0.8 | 5.3 | 0.8 | 4.1 | 0.8 | 3 | 4.3 | 0.8 | 2.9(3) | ns |

**NOTES:**
1. See TEST CIRCUITS AND WAVEFORMS. $T_A$ = -40°C to +85°C.
2. Propagation delay is symmetrical A-B, depending only on input and output $V_{DD}$.
3. Enable/Disable to xAx depends on $V_{DDA}$ only. Times for xBx same if $V_{DDA}$ = $V_{DDB}$.

# TEST CIRCUITS AND WAVEFORMS

| Symbol | $V_{DDX}$(1) = 0.8V | $V_{DDX}$(1) = 1.2V±0.1V | $V_{DDX}$(1) = 1.5V±0.1V | $V_{DDX}$(1) = 1.8V±0.15V | $V_{DDX}$(1) = 2.5V±0.2V | Unit |
|---|---|---|---|---|---|---|
| $V_{LOAD}$ | 2x$V_{DDX}$(1) | 2x$V_{DDX}$(1) | 2x$V_{DDX}$(1) | 2x$V_{DDX}$(1) | 2x$V_{DDX}$(1) | V |
| $V_T$ | $V_{DDX}$/2(1) | $V_{DDX}$/2(1) | $V_{DDX}$/2(1) | $V_{DDX}$/2(1) | $V_{DDX}$/2(1) | V |
| $V_{LZ}$ | 100 | 100 | 100 | 100 | 150 | mV |
| $V_{HZ}$ | 100 | 100 | 100 | 100 | 150 | mV |
| $R_L$ | 2 | 2 | 2 | 1 | 0.5 | kΩ |
| $C_L$ | 15 | 15 | 15 | 30 | 30 | pF |

**NOTE:**
1. Where $V_{DDX}$ refers to either $V_{DDA}$ or $V_{DDB}$.



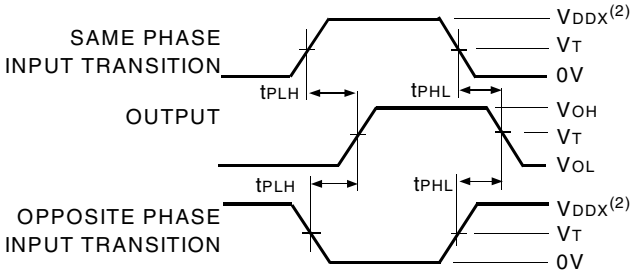

***Test Circuits for All Outputs***

**DEFINITIONS:**
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

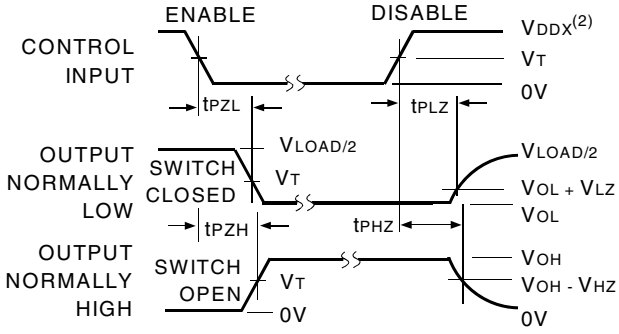
**NOTE:**
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; Slew Rate ≥ 1V/ns.

# SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | $V_{LOAD}$ |
| Disable High<br>Enable High | GND |
| All Other Tests | Open |



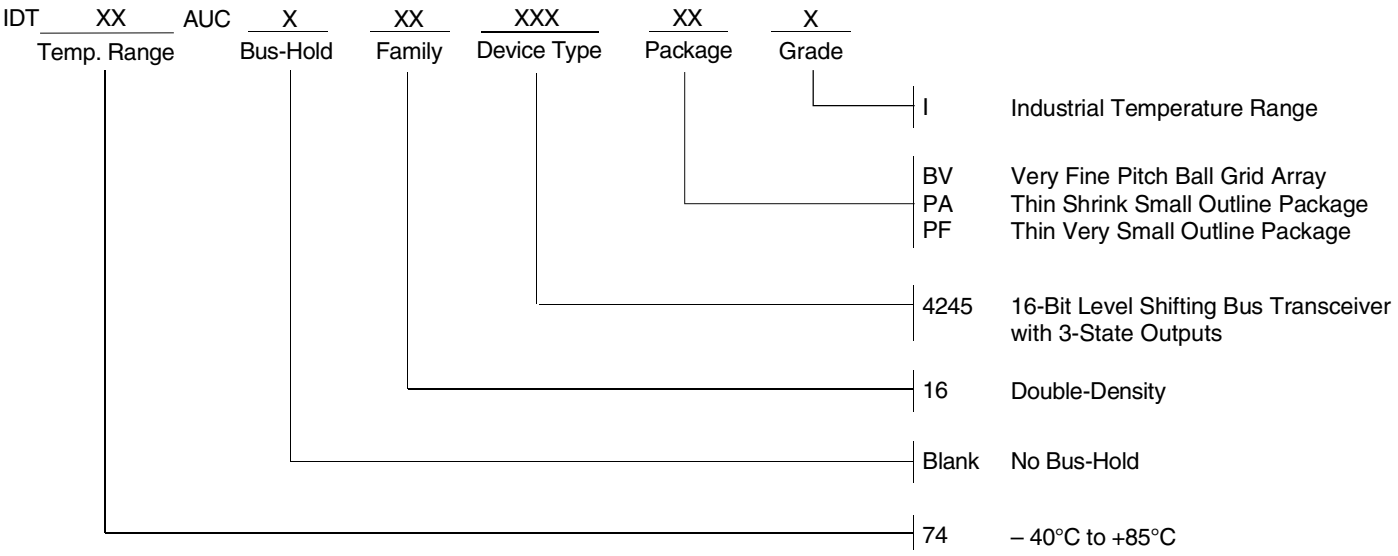

***Propagation Delay***




**NOTES:**
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Where $V_{DDX}$ refers to either $V_{DDA}$ or $V_{DDB}$

***Enable and Disable Times***

## ORDERING INFORMATION

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