1.1 Scope.

This specification covers the detail requirements for two monolithic CMOS analog switches, each consisting of four independent single-pole single-throw switches and latched digital inputs with a WR signal for microprocessor interfacing. They differ only in that the digital control logic is inverted.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	ADG221T(X)/883B
−2	ADG222T(X)/883B

NOTE
[1]To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Terminal LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C)

V+ to V− 44V
V+ to GND 25V
V− to GND . . . . . −25V
Analog Inputs
  Voltage at S, D . . . . . V− to V+
  Continuous Current, S or D 30mA
  Pulsed Current S or D
    1ms Duration, 10% Duty Cycle 70mA
Digital Inputs
  Voltages at IN, WR . . . . . V− −2V to V+ +2V or 20mA, Whichever Occurs First
Power Dissipation (Package)
  Up to +75°C . . . . . 900mW/°C
  Derates above +75°C by . . . . . 12mW/°C
Operating Temperature . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C
Junction Temperature (T_J) . . . . . +175°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-16 and E-20A
θ_{JA} = 120°C/W for Q-16 and E-20A

ADG221/ADG222—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Test Condition[1]/Comments	Units
Switch "ON" Resistance	R_{DS}	– 1, 2	145	90	145	V_{IN} = 0.8V for – 1 Device and 2.4V for – 2 Device; V_D ± 10V, I_S = ∓1.0mA (See Figure 1)	Ω max
		– 1, 2	200	200	200	V + = 10V, V – = 10V; V_D = ± 7.5V; V_{IN} = 0.8V for – 1 Device and 2.4V for – 2 Device; I_S = + 10.0mA (See Figure 1)	Ω max
Source "OFF" Leakage Current	I_S (OFF)	– 1, 2	100	1	100	V_D = ± 14V, V_S = ∓14V; V_{IN} = 2.4 for – 1 Device and 0.8V for – 2 Device, (See Figure 2)	± nA max
Drain "OFF" Leakage Current	I_D (OFF)	– 1, 2	100	1	100	V_D = ± 14V, V_S = ∓14V; V_{IN} = 2.4 for – 1 Device and 0.8V for – 2 Device, (See Figure 3)	± nA max
Channel "ON" Leakage Current	I_D (ON)	– 1, 2	200	1	200	V_D = ± 14V, All Other Digital Inputs = 0.8V for – 1 Device and 2.4V for – 2 Device (See Figure 4)	± nA max
Digital Input High Voltage	V_{INH}	– 1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	– 1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	– 1, 2	1.0	0.5	1.0	V_{IN} = 15V; All Other Digital Inputs = 0.8V (See Figure 5)	± μA max
Low Level Input Current	I_{INL}	– 1, 2	1.0	0.5	1.0	V_{IN} = 0.8V; All Other Digital Inputs = 2.4V (See Figure 5)	± μA max
Supply Current	+ I_{CC}	– 1, 2	2.0	1.5	2.0	V_{IN} = 0V or 5V For All Digital Inputs S1 . . . S4 = D1 . . . D4 = Open Circuit (See Figure 6)	mA max
	– I_{CC}	– 1, 2	2.0	1.5	2.0	V_{IN} = 0V or 5.0V For All Digital Inputs S1 . . . S4 = D1 . . . D4 = Open Circuit (See Figure 6)	mA max
Subgroup 9: T_A = + 25°C							
Write Pulse Width	t_{WR}	– 1, 2	100			(See Paragraph 5.0)	ns min
Digital Input Setup Time	t_{DS}	– 1, 2	100			(See Paragraph 5.0)	ns min
Digital Input Hold Time	t_{HS}	– 1, 2	20			(See Paragraph 5.0)	ns min
Turn "ON" Time	$t_{(ON)}$	– 1, 2	600			C_L = 100pF, R_L = 1k (See Figure 7)	ns max
Turn "OFF" Time	$t_{(OFF)}$	– 1, 2	500			C_L = 100pF; R_L = 1k (See Figure 7)	ns max
Subgroup 10: T_A = + 125°C							
Write Pulse Width	t_{WR}	– 1, 2	120			(See Paragraph 5.0)	ns min
Digital Input Setup Time	t_{DS}	– 1, 2	120			(See Paragraph 5.0)	ns min
Digital Input Hold Time	t_{HS}	– 1, 2	20			(See Paragraph 5.0)	ns min
Turn "ON" Time	$t_{(ON)}$	– 1, 2	800			C_L = 100pF, R_L = 1k (See Figure 7)	ns max
Turn "OFF" Time	$t_{(OFF)}$	– 1, 2	650			C_L = 100pF; R_L = 1k (See Figure 7)	ns max
Subgroup 11: T_A = – 55°C							
Write Pulse Width	t_{WR}	– 1, 2	120			(See Paragraph 5.0)	ns min
Digital Input Setup Time	t_{DS}	– 1, 2	120			(See Paragraph 5.0)	ns min
Digital Input Hold Time	t_{HS}	– 1, 2	20			(See Paragraph 5.0)	ns min
Turn "ON" Time	$t_{(ON)}$	– 1, 2	600			C_L = 100pF, R_L = 1k (See Figure 7)	ns max
Turn "OFF" Time	$t_{(OFF)}$	– 1, 2	500			C_L = 100pF; R_L = 1k (See Figure 7)	ns max
Subgroup 12; T_A = + 25°C Off Isolation	V_{ISO}	– 1, 2	60			f = 200kHz V_{GEN} = 1V p-p; R_L = 1k (See Figure 8)	dB min
Subgroup 13; T_A = + 25°C Crosstalk between Channels	V_{CT}	– 1, 2	60			f = 200kHz V_{GEN} = 1V p-p; R_L = 1k (See Figure 9)	dB min
Subgroup 14; T_A = + 25°C Charge Transfer Error	V_{CTE}	– 1, 2	10			(See Figure 10)	± mV max
Capacitance: Address	C_A	– 1, 2	15			T_A = + 25°C; GND = 0V; f = 1MHz; V_{IN} = 0V	pF max
Capacitance: Input Switch	C_{IS}	– 1, 2	15			T_A = + 25°C; GND = 0V; f = 1MHz; V_{IN} = 5V	pF max
Capacitance: Output Switch	C_{DS}	– 1, 2	20			T_A = + 25°C; GND = 0V; f = 1MHz; V_{IN} = 5V	pF max

NOTE
[1]Unless otherwise noted V + = + 15V; V – = – 15V.

Table 2. Electrical Test Requirements

MIL-STD-883 Test Requirements	Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In) Method 5004	1
Final Electrical Parameters, Method 5004	1*, 2, 3, 9
Group A Electrical Parameters, Method 5005	1, 2, 3, 9, 10, 11
Group C End Point Electrical Parameters, Method 5005	1, 10, 11 and Table 3 Delta Limits

*Indicates P.D.A. applies to Subgroup 1.

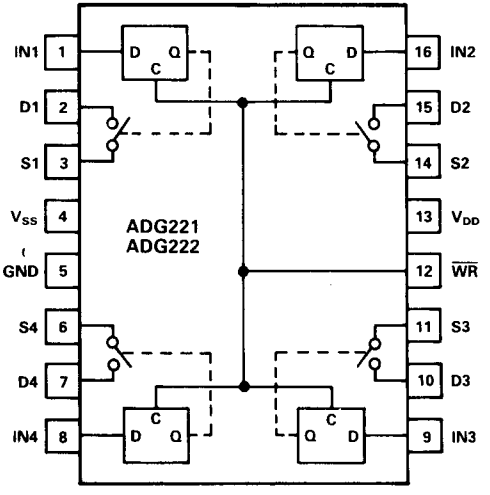
Table 3.

	Delta Limits at +25°C[1] Device Types	
Parameters[2]	1	2
R_{DS}	15Ω	15Ω
I_D(ON)	1nA	1nA

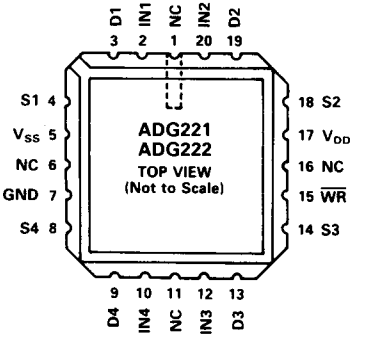
NOTES
[1]Each test applies to every switch in the package.
[2]Each of the above parameters shall be recorded before and after the required burn-in and life-tests to determine deltas (Δ).

3.2.1 Functional Block Diagram and Terminal Assignments.

Q Package (Cerdip)



E Package (LCC)

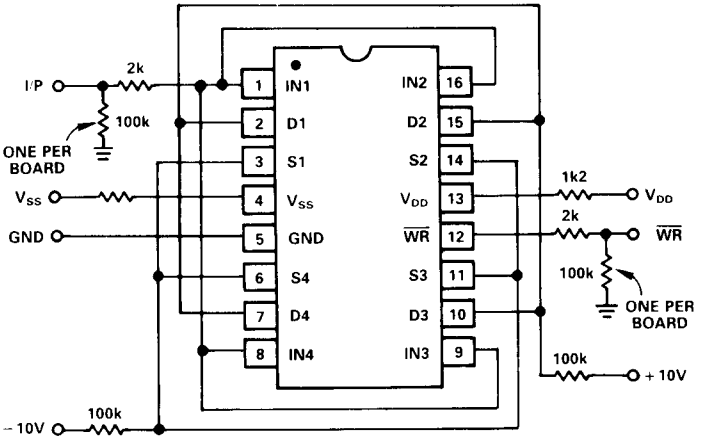


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

4.2.1 Life Test/Burn-In Circuit.

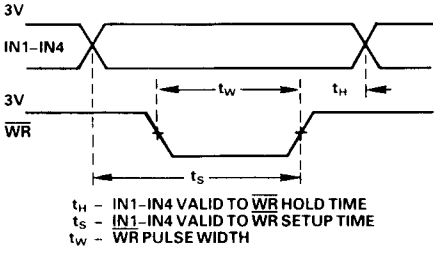
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



I/P = GND
V_{SS} = −15V
V_{DD} = +15V
WR = GND

5.0 Timing and Control Sequence

The diagram below shows the timing sequence for latching the switch digital inputs (IN1–IN4). The latches are level sensitive and, therefore, while $\overline{WR}$ is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.



t_H – IN1–IN4 VALID TO $\overline{WR}$ HOLD TIME
t_S – IN1–IN4 VALID TO $\overline{WR}$ SETUP TIME
t_W – $\overline{WR}$ PULSE WIDTH

Timing and Control Sequence

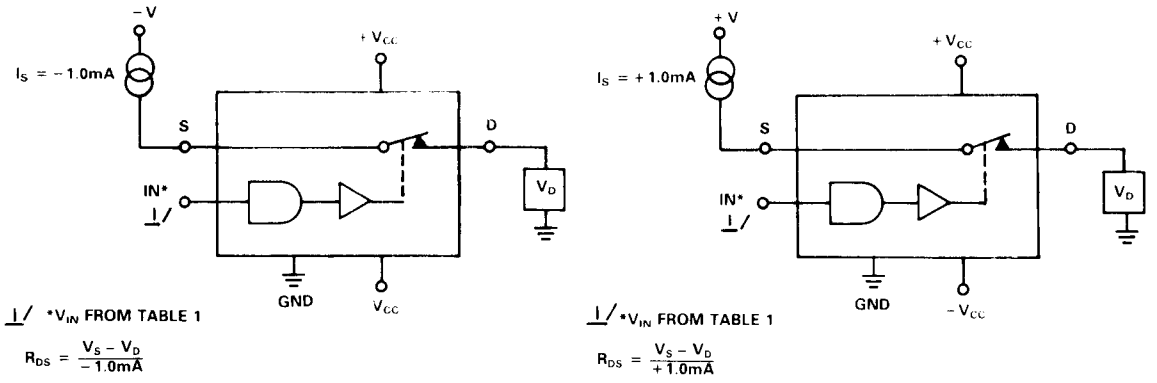


Figure 1. R_{DS} Test Circuits

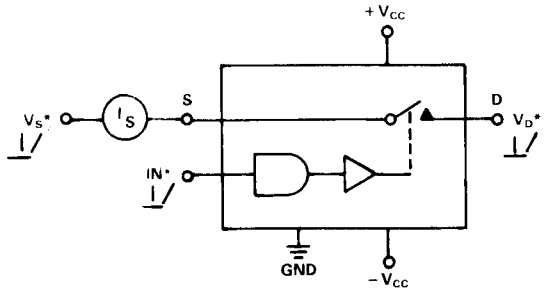


Figure 2. I_S (OFF) Test Circuit

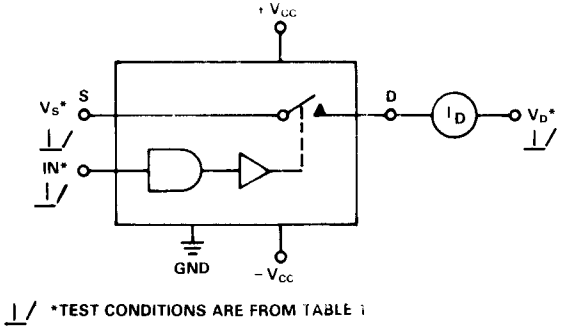


Figure 3. I_D (OFF) Test Circuit

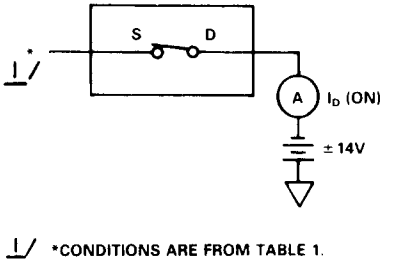
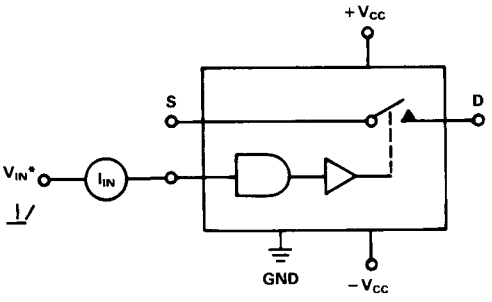


Figure 4. I_D (ON) Test Circuit



1/ *CONDITIONS ARE FROM TABLE 1.

Figure 5. I_{INL}, I_{INH} Test Circuit

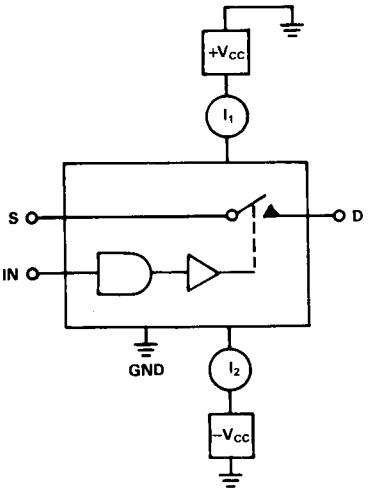
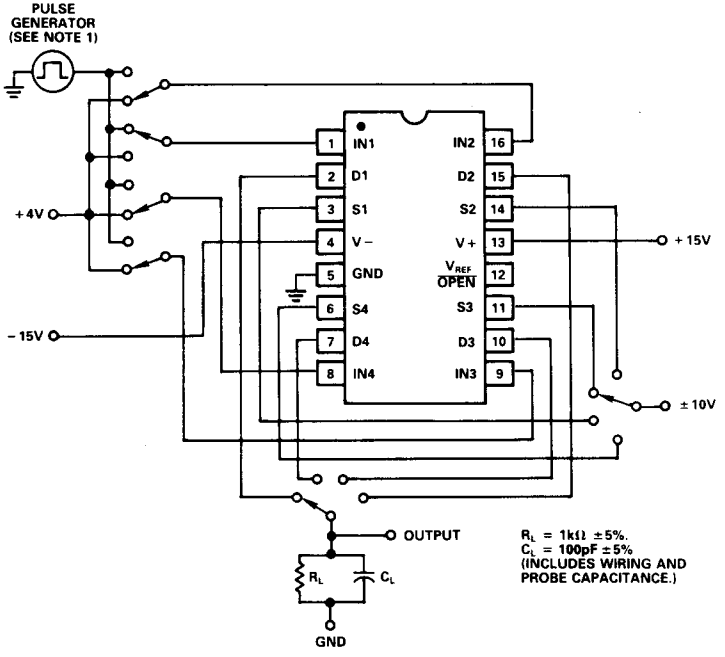
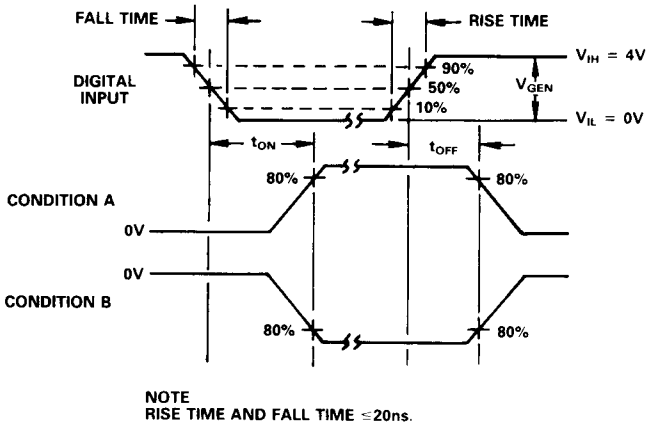


Figure 6. $\pm I_{CC}$ Test Circuit



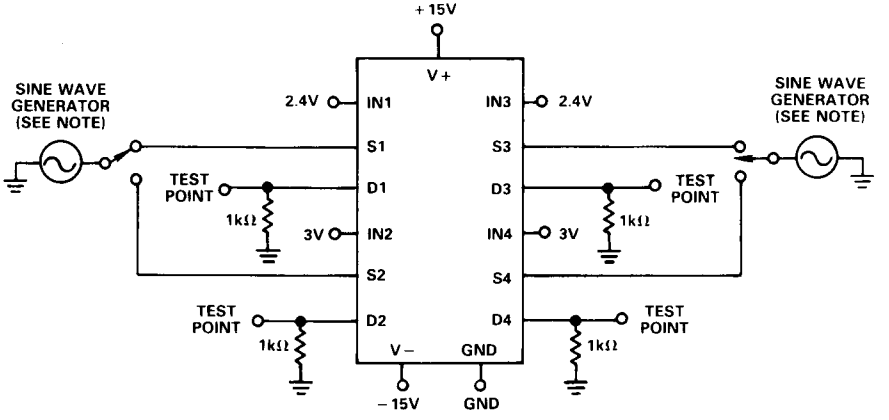
NOTE
1. THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS:
V_{GEN} = 4V, t_{THL} ≤20ns.

Figure 7a. Switching Time Circuits



NOTE
RISE TIME AND FALL TIME ≤20ns.

Figure 7b. Switching Time Waveforms



NOTE
THE SINE WAVE GENERATOR HAS THE FOLLOWING CHARACTERISTICS:
V_{GEN} = 1V p-p, FREQUENCY = 200kHz

Figure 8. Off Isolation Test Circuits

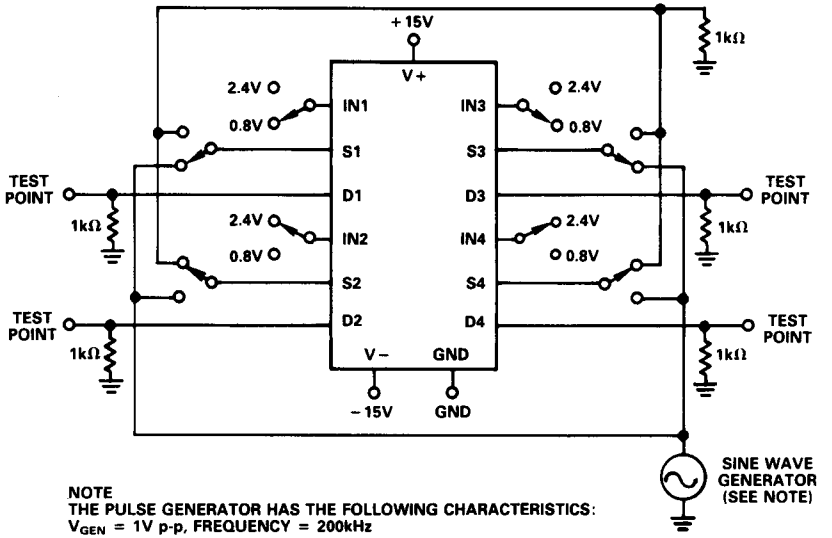


Figure 9. Crosstalk Test Circuit

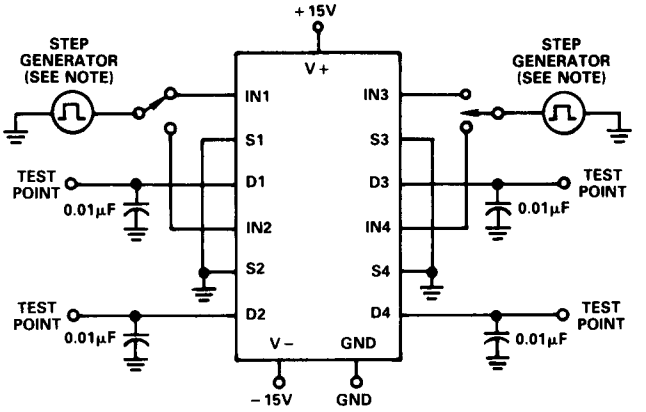


Figure 10. Charge Transfer Error Test Circuits