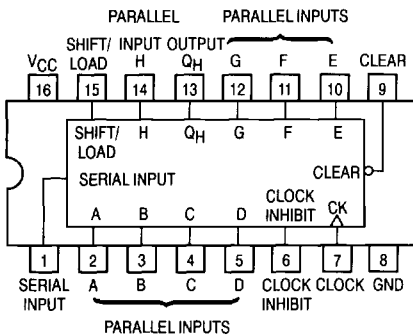


## 8-BIT SHIFT REGISTERS

The SN54L/74LS166 is an 8-Bit Shift Register. Designed with all inputs buffered, the drive requirements are lowered to one 54/74LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified.

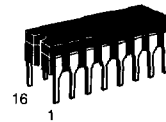
The LS166 is a parallel-in or serial-in, serial-out shift register and has a complexity of 77 equivalent gates with gated clock inputs and an overriding clear input. The shift/load input establishes the parallel-in or serial-in mode. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit function. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A change from low-to-high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

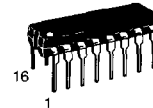


## SN54/74LS166

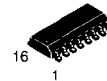
### 8-BIT SHIFT REGISTERS LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08



**D SUFFIX**  
SOIC  
CASE 751B-03

#### ORDERING INFORMATION

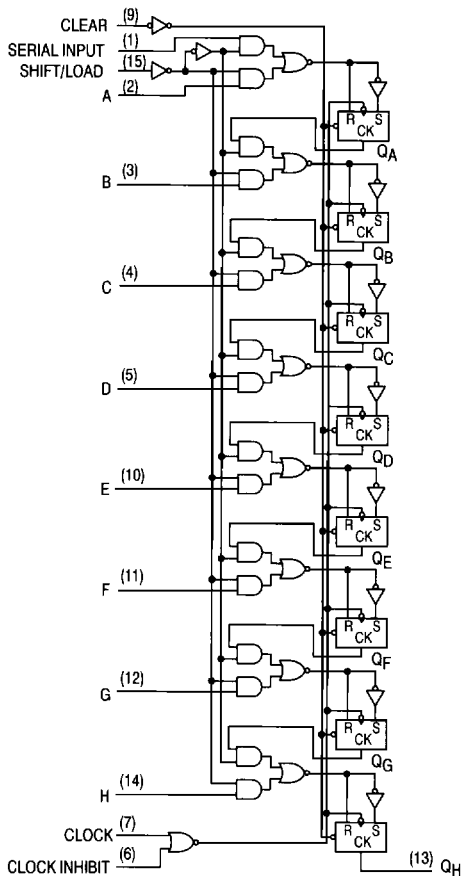
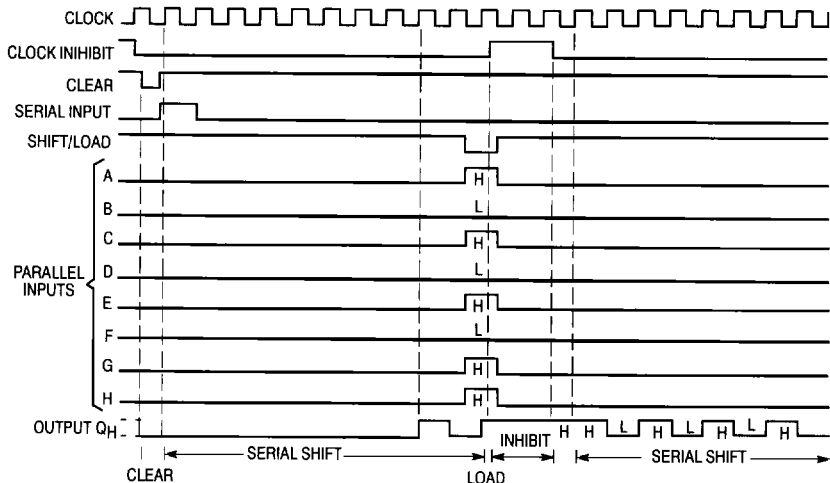
|            |         |
|------------|---------|
| SN54LSXXXJ | Ceramic |
| SN74LSXXXN | Plastic |
| SN74LSXXXD | SOIC    |

FUNCTION TABLE

| INPUTS |                |                  |       |        |          | INTERNAL OUTPUTS |     | OUTPUT<br>QH |
|--------|----------------|------------------|-------|--------|----------|------------------|-----|--------------|
| CLEAR  | SHIFT/<br>LOAD | CLOCK<br>INHIBIT | CLOCK | SERIAL | PARALLEL | QA               | QB  |              |
|        |                |                  |       |        | A...H    | a                | b   |              |
| L      | X              | X                | X     | X      | X        | L                | L   | L            |
| H      | X              | L                | L     | X      | X        | QA0              | QB0 | QH0          |
| H      | L              | L                | ↑     | X      | a...h    | a                | b   | h            |
| H      | H              | L                | ↑     | H      | X        | H                | QAn | QGn          |
| H      | H              | L                | ↑     | L      | X        | L                | QAn | QGn          |
| H      | X              | H                | ↑     | X      | X        | QA0              | QB0 | QH0          |

# SN54/74LS166

## Typical Clear, Shift, Load, Inhibit, and Shift Sequences



# SN54/74LS166

## GUARANTEED OPERATING RANGES

| Symbol          | Parameter                           |          | Min         | Typ        | Max         | Unit |
|-----------------|-------------------------------------|----------|-------------|------------|-------------|------|
| V <sub>CC</sub> | Supply Voltage                      | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V    |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 54<br>74 | -55<br>0    | 25<br>25   | 125<br>70   | °C   |
| I <sub>OH</sub> | Output Current — High               | 54, 74   |             |            | -0.4        | mA   |
| I <sub>OL</sub> | Output Current — Low                | 54<br>74 |             |            | 4.0<br>8.0  | mA   |

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol          | Parameter                      | Limits |       |      | Unit | Test Conditions  |   |
|-----------------|--------------------------------|--------|-------|------|------|--|---|
|                 |                                | Min    | Typ   | Max  |      |  |   |
| V <sub>IH</sub> | Input HIGH Voltage             | 2.0    |       |      | V    | Guaranteed Input HIGH Voltage for All Inputs   |   |
| V <sub>IL</sub> | Input LOW Voltage              | 54     |       | 0.7  | V    | Guaranteed Input LOW Voltage for All Inputs  |   |
|                 |                                | 74     |       | 0.8  |      |  |   |
| V <sub>IK</sub> | Input Clamp Diode Voltage      |        | -0.65 | -1.5 | V    | V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA  |   |
| V <sub>OH</sub> | Output HIGH Voltage            | 54     | 2.5   | 3.5  | V    | V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table |   |
|                 |                                | 74     | 2.7   | 3.5  | V    |  |   |
| V <sub>OL</sub> | Output LOW Voltage             | 54, 74 |       | 0.25 | 0.4  | V  | I <sub>OL</sub> = 4.0 mA<br>V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table |
|                 |                                | 74     |       | 0.35 | 0.5  | V  |   |
| I <sub>IH</sub> | Input HIGH Current             |        |       | 20   | μA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V   |   |
|                 |                                |        |       | 0.1  | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V   |   |
| I <sub>IL</sub> | Input LOW Current              |        |       | -0.4 | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V   |   |
| I <sub>OS</sub> | Short Circuit Current (Note 1) | -20    |       | -100 | mA   | V <sub>CC</sub> = MAX  |   |
| I <sub>CC</sub> | Power Supply Current           |        |       | 38   | mA   | V <sub>CC</sub> = MAX  |   |

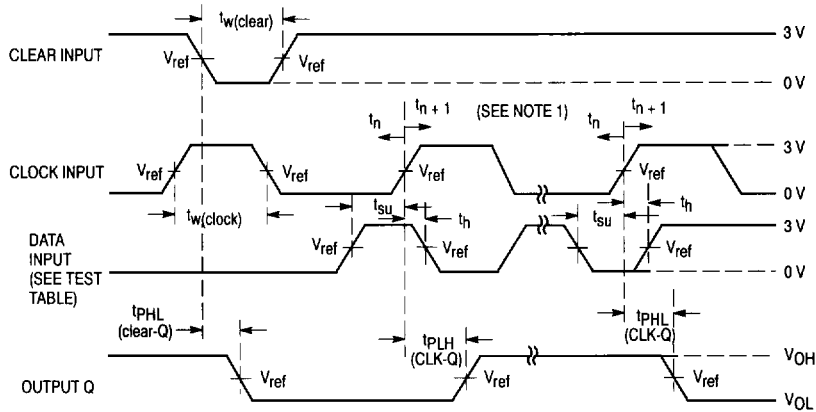
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN54/74LS166

**TEST TABLE FOR SYNCHRONOUS INPUTS**

| DATA INPUT FOR TEST | SHIFT/LOAD | OUTPUT TESTED      |
|---------------------|------------|--------------------|
| H                   | 0 V        | $Q_H$ at $t_{n+1}$ |
| Serial Input        | 4.5 V      | $Q_H$ at $t_{n+8}$ |

**AC WAVEFORMS**



NOTE 1.  $t_n$  = bit time before clocking transition  
 $t_{n+1}$  = bit time after one clocking transition  
 $t_{n+8}$  = bit time after eight clocking transition  
 LS166  $V_{ref}$  = 1.3 V.

**AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )**

| Symbol    | Parameter               | Limits |     |     | Unit | Test Conditions                                   |
|-----------|-------------------------|--------|-----|-----|------|---|
|           |                         | Min    | Typ | Max |      |   |
| $f_{MAX}$ | Maximum Clock Frequency | 25     | 35  |     | MHz  | $V_{CC} = 5.0 \text{ V}$<br>$C_L = 15 \text{ pF}$ |
| $t_{PHL}$ | Clear to Output         |        | 19  | 30  | ns   |   |
| $t_{PLH}$ | Clock to Output         |        | 23  | 35  | ns   |   |

**AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ )**

| Symbol | Parameter               | Limits |     |     | Unit | Test Conditions          |
|--------|-------------------------|--------|-----|-----|------|--------------------------|
|        |                         | Min    | Typ | Max |      |                          |
| $t_w$  | Clock Clear Pulse Width | 30     |     |     | ns   | $V_{CC} = 5.0 \text{ V}$ |
| $t_s$  | Mode Control Setup Time | 30     |     |     | ns   |                          |
| $t_s$  | Data Setup Time         | 20     |     |     | ns   |                          |
| $t_h$  | Hold Time, Any Input    | 15     |     |     | ns   |                          |