MOTOROLA

MC74AC648

Product Preview

Octal Transceiver/Register with 3-State Outputs (Inverting)

OCTAL TRANSCEIVER/REGISTER WITH 3-STATE OUTPUTS (INVERTING)

The MC74AC648 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in the following figures.

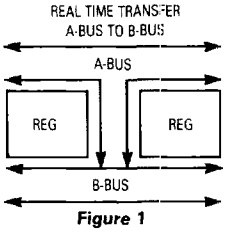


Figure 1

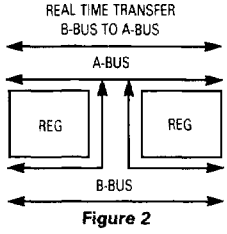


Figure 2

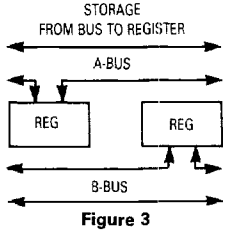


Figure 3

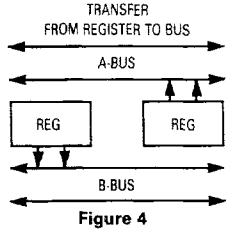
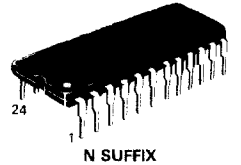
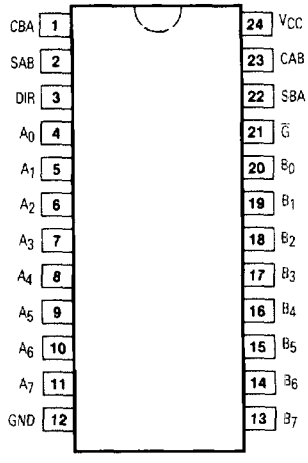


Figure 4



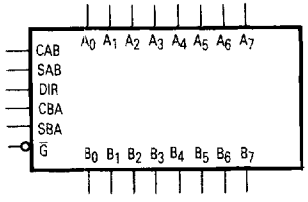
N SUFFIX
CASE 649-03
PLASTIC

DW SUFFIX
CASE 751E-02
PLASTIC



- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data Transfers
- Choice of True and Inverting Data Paths
- 3-State Outputs
- 300 mil Slim Dual In-Line Package
- Outputs Source/Sink 24 mA

LOGIC SYMBOL



PIN NAMES

A_0–A_7	Data Register Inputs
	Data Register A Outputs
B_0–B_7	Data Register B Inputs
	Data Register B Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

5

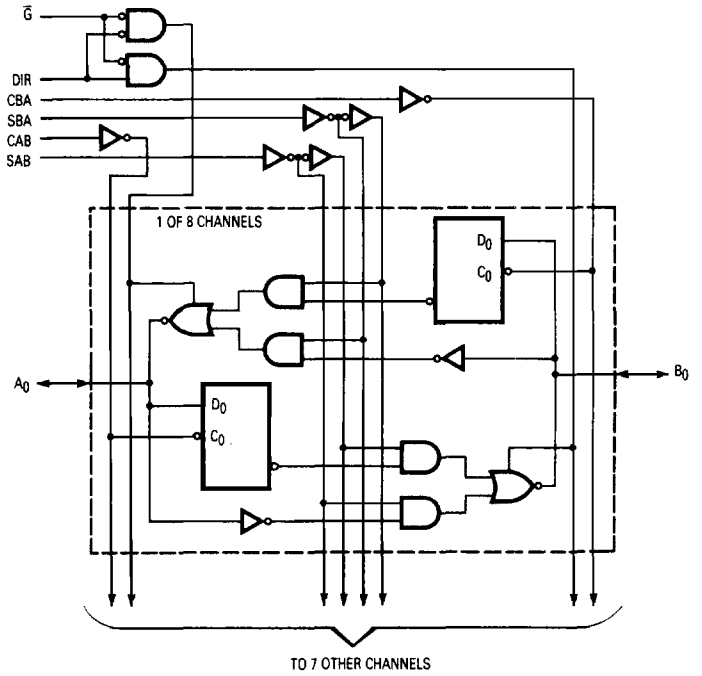
FUNCTION TABLE

Inputs						Data I/O*		Operation or Function
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	⌐	⌐	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus

*The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0	10 7.0	15.5 11	1.0 1.0	17 12	ns	3-6
t_{PHL}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0	8.5 6.0	13.5 10.5	1.0 1.0	14.5 11.5	ns	3-6
t_{PLH}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0	6.0 4.0	10 7.0	1.0 1.0	11 7.5	ns	3-5
t_{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0	5.5 3.5	9.0 7.5	1.0 1.0	10 8.0	ns	3-5
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0	1.0 1.0	14 10	ns	3-6
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.5	1.0 1.0	14 10.5	ns	3-6
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	6.5 5.0	11 8.0	1.0 1.0	11.5 9.0	ns	3-7
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.0	11 8.0	1.0 1.0	12.5 9.0	ns	3-8
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.5 6.0	12 10	1.0 1.0	13 11	ns	3-7
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	12.5 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS — continued (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PZH}	Enable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	6.0 4.5	12.5 9.5	1.0 1.0	14 10.5	ns	3-7
t_{PZL}	Enable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	6.5 4.5	13 9.0	1.0 1.0	14.5 10.5	ns	3-8
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	13.5 10	ns	3-7
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.0 50	13.5 9.5	1.0 1.0	15 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup time, HIGH or LOW Bus to Clock	3.3 5.0	2.0 1.5	3.0 2.0	3.5 2.0	ns	3-9
t_h	Hold Time, HIGH or LOW Bus to Clock	3.3 5.0	−1.5 −0.5	0 1.0	0 1.0	ns	3-9
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	2.0 2.0	3.5 3.0	4.0 3.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
$C_{I/O}$	Input/Output Capacitance	15	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	65	pF	V_{CC} = 5.0 V

5