20-BIT BUS SWITCH

IDT74FST32XL2384

FEATURES:

– Bus switches provide zero delay paths
– Extended commercial range of –40°C to +85°C
– Low switch on-resistance: FST32XL2384 – 28Ω
– TTL-compatible input and output levels
– ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
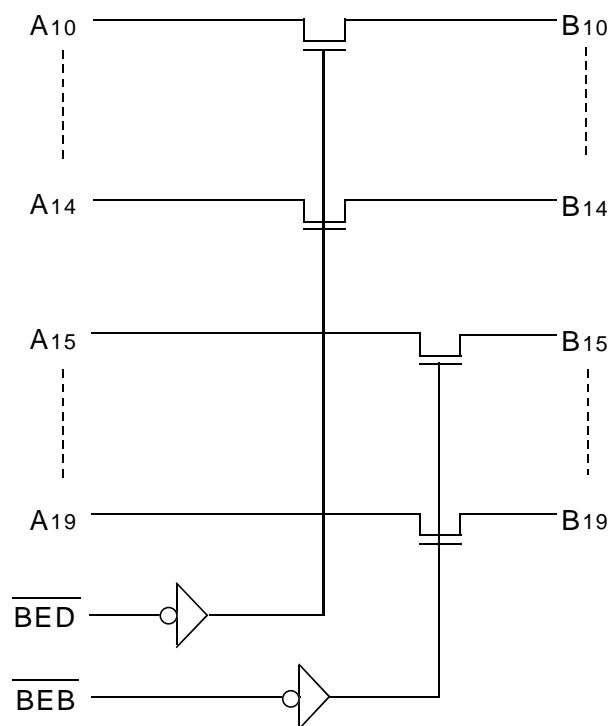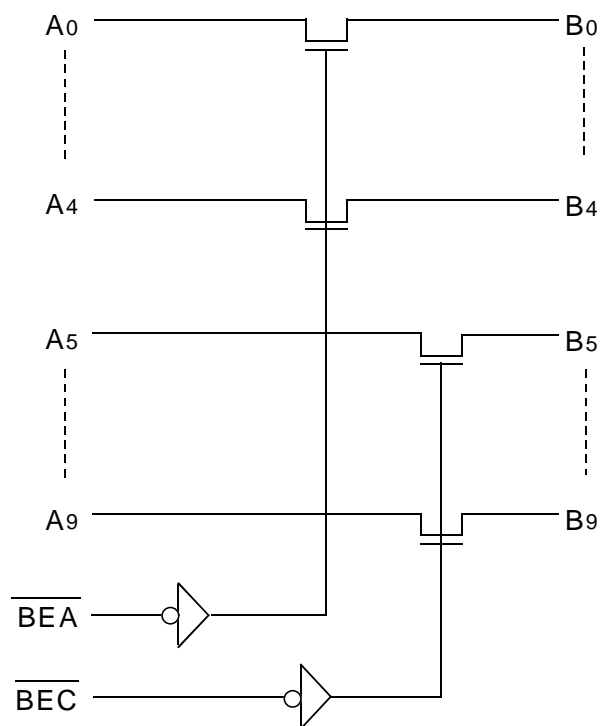– Available in SSOP, TSSOP, and TVSOP Packages

DESCRIPTION:

The FST32XL2384 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no V_{CC} applied, the device has hot insertion capability.
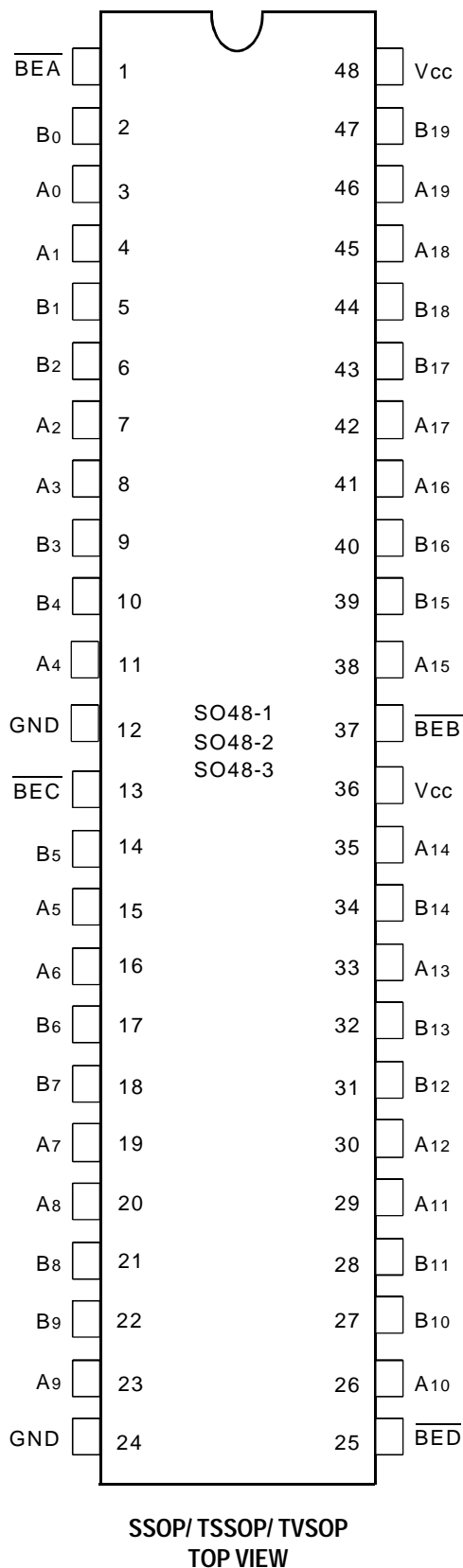
The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST32XL2384 is a 20-bit TTL-compatible bus switch. The BEx pins provide enable control.

FUNCTIONAL BLOCK DIAGRAM

EXTENDED COMMERCIAL TEMPERATURE RANGE

SEPTEMBER 1999

PIN CONFIGURATION

$\overline{BEA}$	1	48	Vcc
B0	2	47	B19
A0	3	46	A19
A1	4	45	A18
B1	5	44	B18
B2	6	43	B17
A2	7	42	A17
A3	8	41	A16
B3	9	40	B16
B4	10	39	B15
A4	11	38	A15
GND	12	37	$\overline{BEB}$
$\overline{BEC}$	13	36	Vcc
B5	14	35	A14
A5	15	34	B14
A6	16	33	A13
B6	17	32	B13
B7	18	31	B12
A7	19	30	A12
A8	20	29	A11
B8	21	28	B11
B9	22	27	B10
A9	23	26	A10
GND	24	25	$\overline{BED}$

SO48-1
SO48-2
SO48-3

SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Max.	Unit
VTERM[2]	Terminal Voltage with Respect to GND	–0.5 to +7	V
TSTG	Storage Temperature	–65 to +150	°C
IOUT	Maximum Continuous Channel Current	128	mA

FST LINK

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc, Control, and Switch terminals.

CAPACITANCE [1]

Symbol	Parameter	Conditions[2]	Typ.	Unit
CIN	Control Input Capacitance		4	pF
CI/O	Switch Input/Output Capacitance	Switch Off	8	pF

NOTES:
1. Capacitance is characterized but not tested.
2. $T_A = 25°C$, f = 1MHz, $V_{IN} = 0V$, $V_{OUT} = 0V$

PIN DESCRIPTION

Pin Names	I/O	Description
A19-A0	I/O	Bus A
B19-B0	I/O	Bus B
$\overline{BEA}$	I	Enable, 0-4
$\overline{BEB}$	I	Enable, 15-19
$\overline{BEC}$	I	Enable, 5-9
$\overline{BED}$	I	Enable, 10-14

FUNCTION TABLE[1]

$\overline{BEA}$	$\overline{BEB}$	B0-B4	B15-B19	Description
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A0-A4	Hi-Z	Connect
H	L	Hi-Z	A15-A19	Connect
L	L	A0-A4	A15-A19	Connect
$\overline{BEC}$	**$\overline{BED}$**	**B5-B9**	**B10-B14**	**Description**
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A5-A9	Hi-Z	Connect
H	L	Hi-Z	A10-A14	Connect
L	L	A5-A9	A10-A14	Connect

NOTE:
1. H = HIGH
   L = LOW
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Conditions: T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance[4]	V_{CC} = Min. V_{IN} = 0.0V I_{ON} = 30mA		20	28	40	Ω
		V_{CC} = Min. V_{IN} = 2.4V I_{ON} = 15mA		20	35	48	Ω
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \le$ 4.5V		—	—	1	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.1	3	µA

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	30	40	µA/ MHz/ Switch
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Enable Pins Toggling (20 Switches Toggling) f_i = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	6	8	mA
			V_{IN} = 3.4 V_{IN} = GND	—	7	11	

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} ($f_i N$)
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Input Frequency
   N = Number of Switches Toggling at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Conditions: T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Description	Condition[1]	Min.[2]	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay Ai to Bi, Bi to Ai[3,4]	C_L = 50pF R_L = 500Ω	—	—	1.25	ns
t_{PZH} t_{PZL}	Switch Turn on Delay BEx to Ai, Bi		1.5	—	7.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay BEx to Ai, Bi[3]		1.5	—	5.5	ns
$\lvert Q_{CI}\rvert$	Charge Injection[5,6]		—	1.5	—	pC

NOTES:

1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 2.5ns for 50pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay on the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50pF in parallel with 10MΩ scope probe, V_{IN} = 0.0 volts.
6. Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS

V CC

7.0V

500Ω

Pulse Generator — V IN — D.U.T. — V OUT

50pF

R T

C L

500Ω

Octal link
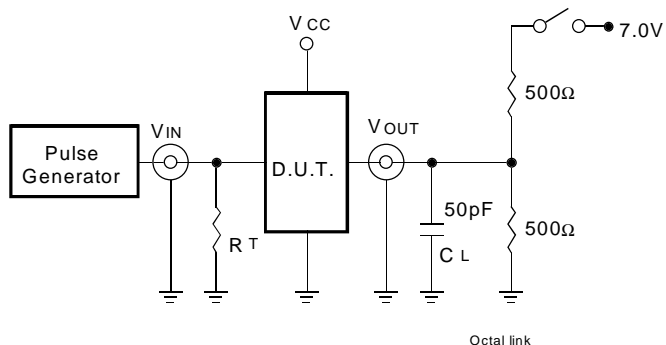
SWITCH POSITION

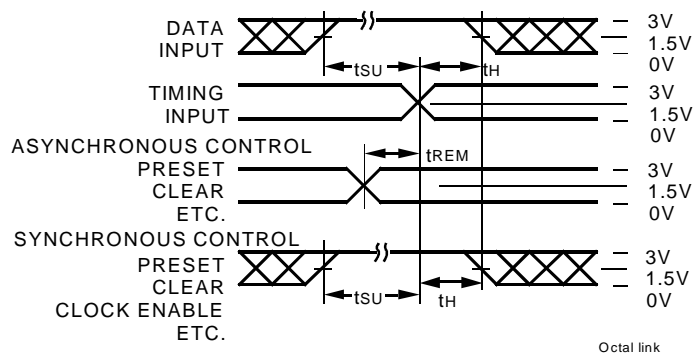| Test	Switch
Open Drain	
Disable Low	Closed
Enable Low	
All Other Tests	Open

FCT LINK

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
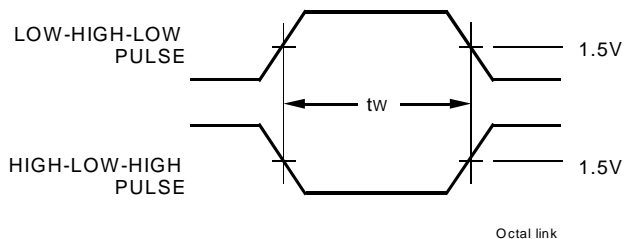R_T = Termination resistance: should be equal to Z_OUT of the Pulse Generator.
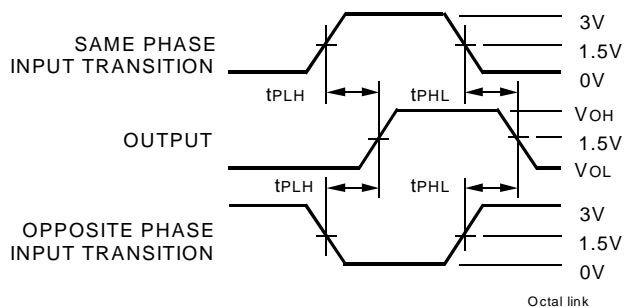
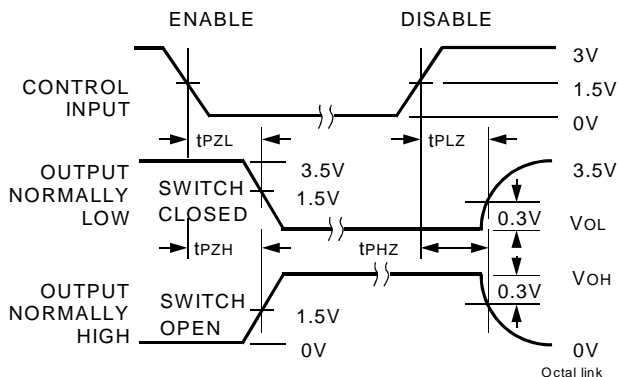## SET-UP, HOLD, AND RELEASE TIMES

DATA INPUT — 3V 1.5V 0V
t_{SU} t_H
TIMING INPUT — 3V 1.5V 0V
ASYNCHRONOUS CONTROL
PRESET CLEAR ETC. — t_{REM} — 3V 1.5V 0V
SYNCHRONOUS CONTROL
PRESET CLEAR CLOCK ENABLE ETC. — t_{SU} t_H — 3V 1.5V 0V

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PULSE WIDTH

LOW-HIGH-LOW PULSE — 1.5V
t_W
HIGH-LOW-HIGH PULSE — 1.5V

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PROPAGATION DELAY

SAME PHASE INPUT TRANSITION — 3V 1.5V 0V
t_{PLH} t_{PHL}
OUTPUT — V_OH 1.5V V_OL
t_{PLH} t_{PHL}
OPPOSITE PHASE INPUT TRANSITION — 3V 1.5V 0V

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ENABLE AND DISABLE TIMES

ENABLE   DISABLE
CONTROL INPUT — 3V 1.5V 0V
t_{PZL} t_{PLZ}
OUTPUT NORMALLY LOW — SWITCH CLOSED 3.5V 1.5V — 3.5V 0.3V V_OL
t_{PZH} t_{PHZ}
OUTPUT NORMALLY HIGH — SWITCH OPEN 1.5V 0V — V_OH 0.3V 0V

Octal link

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION

IDT   <u>XX</u>   FST   <u>XXXXXXX</u>   <u>XX</u>
      Temp. Range   Device Type   Package

PV	Shrink Small Outline Package (SO48-1)
PA	Thin Shrink Small Outline Package (SO48-2)
PF	Thin Very Small Outline Package (SO48-3)

32XL2384	20-Bit Bus Switch

74	−40°C to +85°C