



MM54HCT174/MM74HCT174 Hex D Flip-Flops with Clear

General Description

The MM54HCT174/MM74HCT174 utilize 3.0 micron N-well microCMOS technology. They have input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These positive edge-triggered flip-flops have a common clock and clear and independent Q outputs. Data on a D input, having the specified set-up and hold time, is transferred to the corresponding Q output on the positive-going transition of the clock pulse. The asynchronous clear forces all outputs low when it is low.

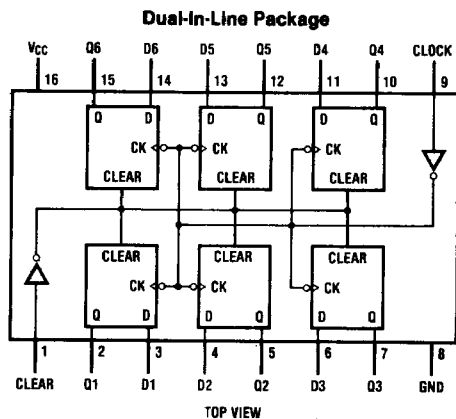
All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. When there is a LS-TTL equivalent, these parts can be used as plug-in replacements to reduce system power consumption in existing designs.

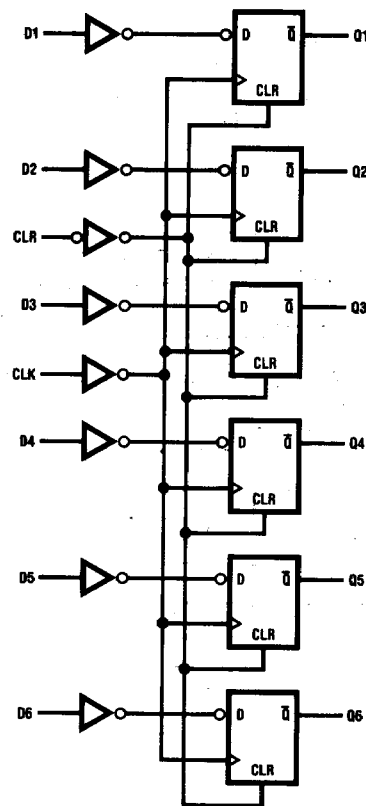
Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μ A maximum (74HCT series)
- Fanout of 10 LS-TTL loads

Connection Diagram



Logic Diagram



Truth Table (Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

H = high level (steady-state)

L = low level (steady-state)

X = don't care

↑ = transition from low to high level

Q0 = the level of Q before the indicated steady-state input conditions were established.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	- 0.5V to + 7.0V
DC Input Voltage (V_{IN})	- 1.5V to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	- 0.5V to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per Pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	- 65°C to + 150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	- 40	+ 85	°C
MM54HCT	- 55	+ 125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ unless otherwise specified

Symbol	Parameter	Conditions	$T_A = 25^\circ C$			Units
			Typ	74HCT $T_A = -40^\circ C$ to $85^\circ C$	54HCT $T_A = -55^\circ C$ to $125^\circ C$	
V_{IH}	Minimum High Level Input Voltage		2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage		0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} = 20 \mu A$	V_{CC}	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$
		$ I_{OUT} = 4.0$ mA, $V_{CC} = 4.5V$	4.2	3.98	3.84	3.7
		$ I_{OUT} = 4.8$ mA, $V_{CC} = 5.5V$	5.7	4.98	4.84	4.7
V_{OL}	Maximum Low Level Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} = 20 \mu A$	0	0.1	0.1	0.1
		$ I_{OUT} = 4.0$ mA, $V_{CC} = 4.5V$	0.2	0.26	0.33	0.4
		$ I_{OUT} = 4.8$ mA, $V_{CC} = 5.5V$	0.2	0.26	0.33	0.4
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL}	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	8	80	160	μA
		$V_{IN} = 2.4V$ or $0.5V$ (Note 4)				mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: - 12 mW/°C from 65°C to 85°C; ceramic "J" package: - 12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25^\circ C, C_L = 15$ pF, $t_r = t_f = 6$ ns (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		18	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock			20	ns
t_S	Minimum Set-Up Time D to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Q		- 3	0	ns
t_W	Minimum Pulse Width Clock or Clear		8	16	ns

AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$, $C_L = 50 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$ unless otherwise specified

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		74HCT	54HCT	Units
			Typ	Guaranteed Limits		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		22	35	44	52	ns
t_{REM}	Minimum Removal Time Clear to Clock			20	25	30	ns
t_S	Minimum Set-Up Time D to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to D		-3	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear			16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.