

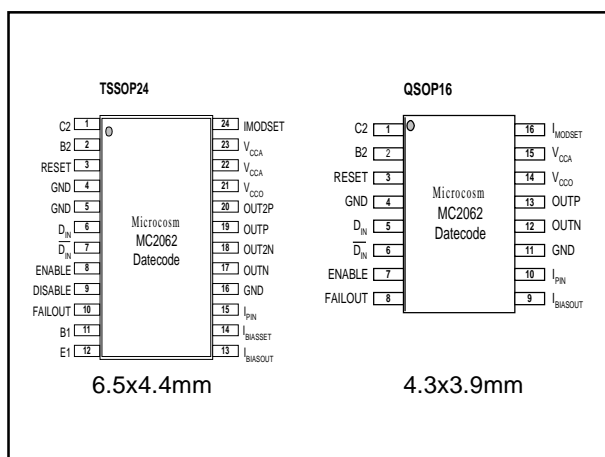
FEATURES

- ❑ Low-cost IC, fabricated in advanced sub-micron BiCMOS process
- ❑ Designed for driving VCSELs and low current Fabry Perot lasers
- ❑ Very wide range of operation; suitable for <100Mbps to 1.25Gbps applications
- ❑ Rise/fall times <250ps
- ❑ Independently programmable VCSEL bias and modulation currents
- ❑ Bias current up to 20mA and modulation current up to 40mA at $V_{CC}=3.3V$
- ❑ Open and closed loop configuration
- ❑ Operates with standard 5V or 3.3 V supply ($\pm 10\%$)
- ❑ The MC2062 is available in TSSOP24 and QSOP16 packages, or in die form

APPLICATIONS

- ❑ Gigabit Ethernet
- ❑ Fiber Channel 100
- ❑ Fast Ethernet

CONNECTIONS



DESCRIPTION

The MC2062 is a highly integrated, programmable laser driver for fiber optic communications systems operating at up to 1.25Gbps. Both 3.3V and 5V operation are supported.

The MC2062 has differential PECL data inputs and CMOS control inputs. The modulation current and temperature coefficient are programmed by the selection of resistor values. The bias current may be controlled in a servo loop, using a feedback photodetector. Alternatively, the bias current and temperature coefficient may be programmed using external resistors.

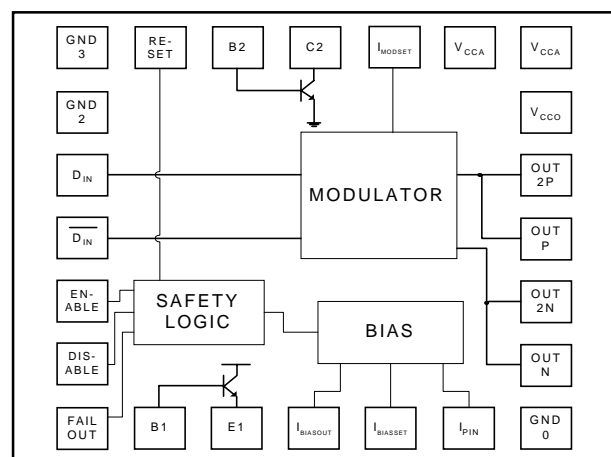
The MC2062 includes circuits to monitor the operation of the bias current control loop and to monitor the power supply level. These are used to control a safety logic function. The safety logic output on the FAILOUT pin indicates when failure of the bias control loop is detected.

On the QSOP16 package, the FAILOUT pin is internally bonded to the DISABLE pad on the die. The output is always disabled when the control loop fails.

ORDERING INFORMATION

Part	Pin-Package
MC2062DIE	Waffle pack
MC2062DIEW	Expanded Whole Wafer on a Ring
MC2062T24	TSSOP24
MC2062T24TR	TSSOP24 Tape and Reel
MC2062Q16	QSOP16
MC2062Q16TR	QSOP16 Tape and Reel

TOP LEVEL DIAGRAM



PIN DESCRIPTION

Pin Name	16 QSOP Pin No.	20 TSSOP Pin No.	Function
C2	1	1	NPN collector. Used in conjunction with B2 for temperature compensation of modulation current.
B2	2	2	NPN base. Used in conjunction with C2 for temperature compensation of modulation current.
RESET	3	3	Value of capacitor connected to this internal resistor determines length of reset pulse to latch.
GND	-	4	Ground pin.
GND	4	5	Ground pin
D _{IN}	5	6	Non-inverted data input. May be AC-coupled or directly coupled to differential PECL source.
\overline{D}_{IN}	6	7	Inverted data input. May be AC-coupled or directly coupled to differential PECL source.
ENABLE	7	8	CMOS logic input. On-chip pull-up.
DISABLE	-	9	CMOS logic input. On-chip pull-down.
FAILOUT	8 ⁽¹⁾	10	Latched safety logic output.
B1	-	11	NPN base. Used in conjunction with E1 for temperature compensation of bias current in open loop operation
E1	-	12	NPN emitter. Used in conjunction with B1 for temperature compensation of bias current in open loop operation.
I _{BIASOUT}	9	13	Bias current output.
I _{BIASSET}	-	14	Reference current output for control of bias current when feedback photodetector is not used.
I _{PIN}	10	15	Control input for bias current control circuit.
GND	11	16	Ground pin.
OUTN	12	17	Modulator output. Draws current when D _{IN} =0.
OUT2N	12	18	Modulator output. Draws current when D _{IN} =0.
OUTP	13	19	Modulator output. Draws current when D _{IN} =1.
OUT2P	13	20	Modulator output. Draws current when D _{IN} =1.
V _{CCO}	14	21	Positive supply for modulator and bias circuit outputs.
V _{CCA}	-	22	Positive supply for circuits other than modulator and bias outputs.
V _{CCA}	15	23	Positive supply for circuits other than modulator and bias outputs.
I _{MODSET}	16	24	Control input for modulation current setting circuit.

¹ Failout is connected to Disable internal to the QSOP16 package. As a result, a fault condition will disable the laser drive circuitry.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
V_{CC}	Power Supply (V_{CC} -Gnd)	6	V
T_A	Operating ambient	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC} -GND)	3 to 5.5	V
T_A	Operating ambient	-40 to +85 ⁽¹⁾	°C

¹ Check with Microcosm for allowable combinations of package/thermal resistance, power supply voltage and drive currents.

AC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units
I_{MODOUT}	Modulation current available at each output	40	-	-	mApp
$I_{MOD}(VCSEL)$	Modulation current into VCSEL $Z_{VCSEL}=50\Omega$ $Z_{VCSEL}=25\Omega$	-	16 26	-	mApp
t_R, t_F	Modulation current rise/fall times (10-90% points) at modulator output pins with loads of 50Ω to positive supply.	-	-	250	ps
TC_{IOUT}	Range of programmable temperature coefficient on modulation current.	-250 ⁽¹⁾	-	>10,000	ppm/°C
t_{PWD}	Modulation current pulse width distortion	-	-	TBD	%
M_{IMOD}	Modulation current multiplier	-	96	-	A/A
C_{IMOD}	Modulation current offset	-	-2	-	mA

¹ This is the value with no external temperature compensation set.

DC CHARACTERISTICS

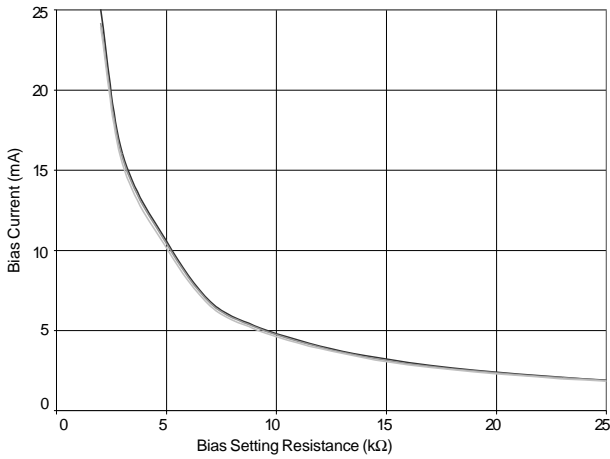
Symbol	Parameter	Min.	Typ.	Max.	Units
R_{IN}	On-chip resistance D_{IN} to $\overline{D_{IN}}$ (for impedance matching to input bond wires)	-	600	-	Ω
$R_{N'}, R_P$	On-chip modulator pull-up resistors. ⁽¹⁾	65	75	85	Ω
V_{IH}	PECL Input High	$V_{CC}-1150$	-	$V_{CC}-800$	mV
V_{IL}	PECL Input Low	$V_{CC}-1900$	-	$V_{CC}-1500$	mV
V_{CIH}	Enable and Disable Input High	-	$0.66 \times V_{CC}$	-	V
V_{CIL}	Enable and Disable Input Low	-	$0.33 \times V_{CC}$	-	V
I_{CC}	Supply current	-	$I_{BIAS}^{MOD} + 14mA$	-	mA
I_{BIAS}	Maximum programmable bias current	20	-	-	mA
$TC_{BIASOUT}$	Range of programmable temperature coefficient on Bias Current (open loop operation)	-1,000 ⁽²⁾	-	>20,000	ppm/°C
V_{SUPTH}	Supply detection threshold.	-	2.4	-	V
V_{REF1}	Voltage ref. used for mod current control	1.15	1.2	1.25	V
V_{REF2}	Voltage ref. used for bias current control	$V_{CCA}-1.25$	$V_{CCA}-1.2$	$V_{CCA}-1.15$	V
V_{REF3}	Upper voltage ref. used to monitor bias control loop.	$V_{CCA}-1.15$	$V_{CCA}-1.1$	$V_{CCA}-1.05$	V
V_{REF4}	Lower voltage ref. used to monitor bias control loop	$V_{CCA}-1.35$	$V_{CCA}-1.3$	$V_{CCA}-1.25$	V
M_{BIAS}	Bias current multiplier	-	39	-	A/A
R_{RESET}	Pull-up resistor connected to RESET pin	400	500	600	k Ω
C_{BIAS}	Bias current offset.	-	-1	-	mA

¹ The value of this on-chip resistor is mask-programmable. Contact Microcosm for details on how to match this value to your desired VCSEL.

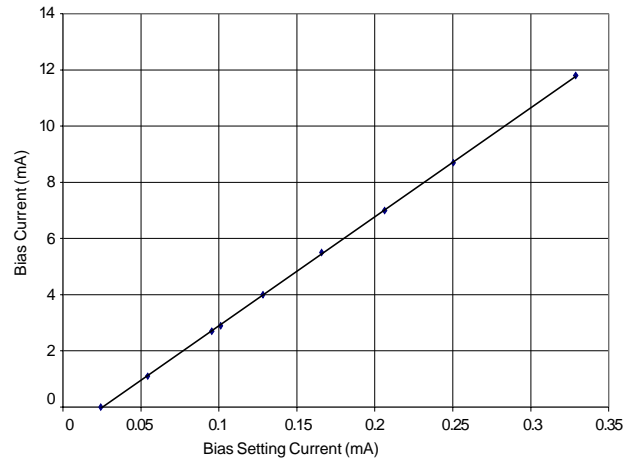
² This is the value with no external compensation set.

TYPICAL PERFORMANCE CURVES

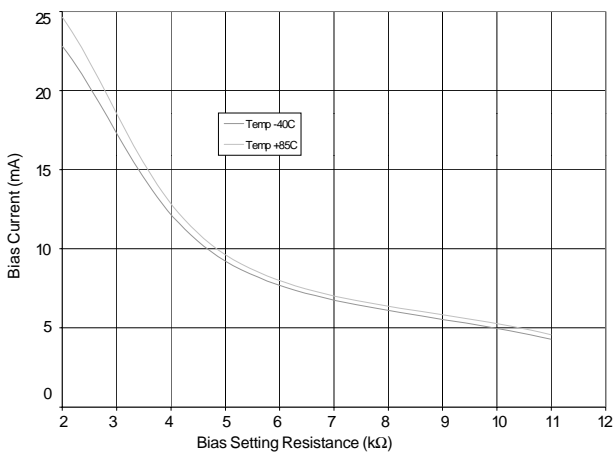
Bias Current vs Bias Setting Resistance



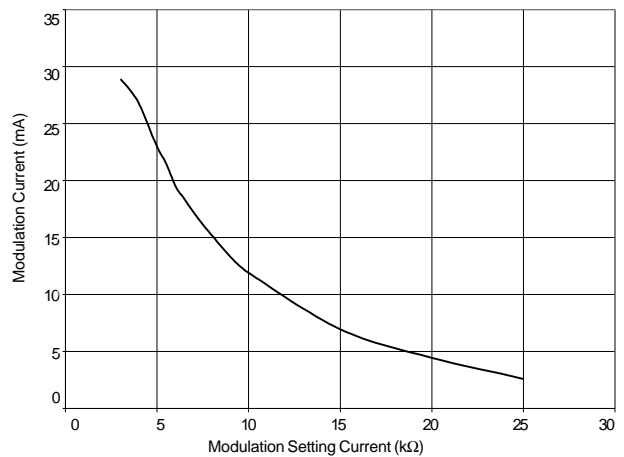
Bias Current vs Bias Setting Current



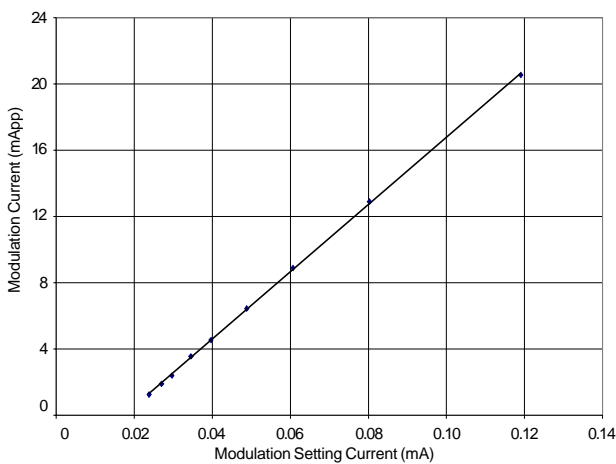
Open Loop Bias Current with Temperature



Modulation Current vs Modulation Setting Resistance

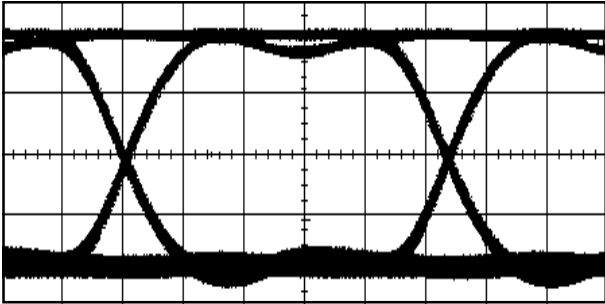


Modulation Current vs Modulation Setting Current

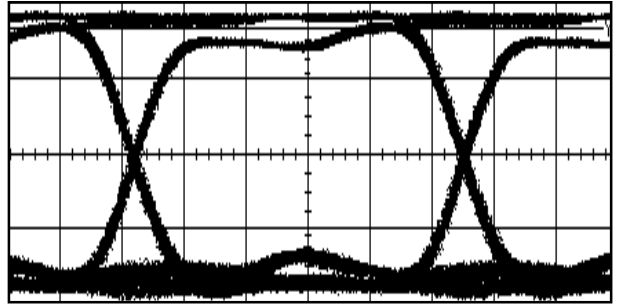


EYE DIAGRAMS

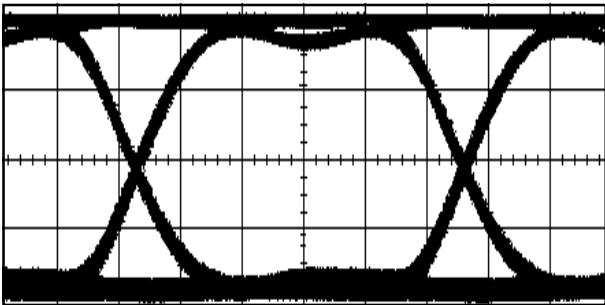
Electrical Eye @ 25°C



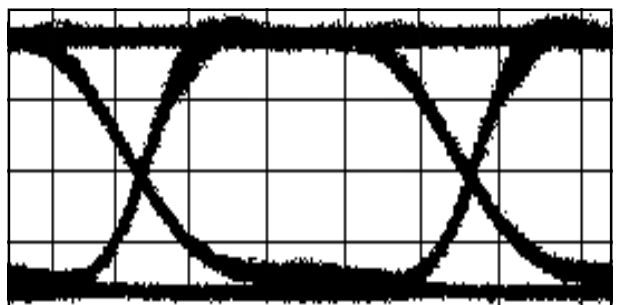
Electrical Eye @ -40°C



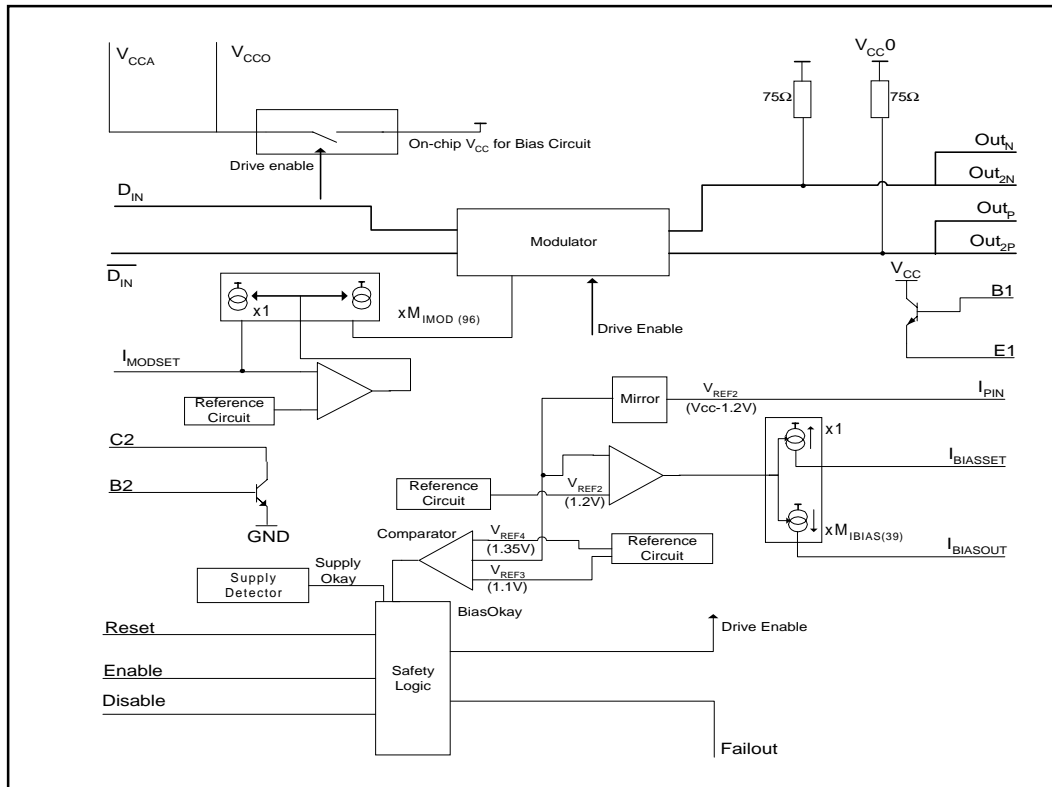
Electrical Eye @ +85°C



Optical Eye (850nm Vcsel)



FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MC2062 VCSEL driver provides a high speed modulator together with the circuits for setting the modulation current, controlling the bias current and for monitoring bias control loop and supply level. CMOS logic inputs may be connected to control the MC2062, and a CMOS output is provided to indicate a detected failure of the bias control loop.

High Speed Modulator

The modulator is connected to the self-biased PECL data inputs (D_{IN} and \overline{D}_{IN}). The modulator steers the modulation current between outputs OUTN/OUT2N and OUTP/OUT2P. The pairs of outputs are identical and are connected in parallel.

The resistors connected to pins I_{MODSET} , C2 and B2 are used to set the modulation current and temperature coefficient of modulation current.

Bias Generator

The first application circuit on page 8 shows how the bias current can be controlled when a feedback photodetector is available (closed loop operation). The

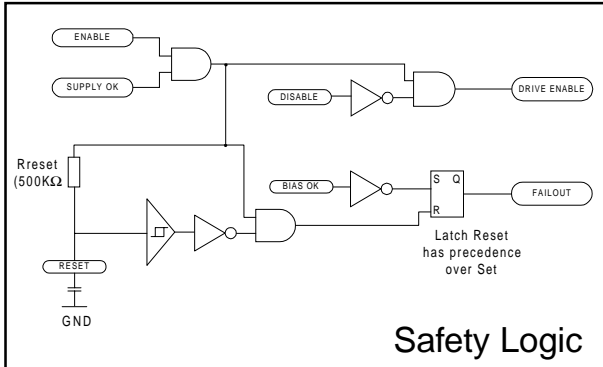
second circuit on page 9 shows the configuration that may be used to achieve the desired bias current and temperature coefficient when a feedback photodiode is not used (open loop). In both cases the voltage at pin I_{PIN} is equal to the voltage V_{REF2} .

A further reference circuit and a window comparator detect whether the voltage at pin I_{PIN} is between the voltages V_{REF3} and V_{REF4} . Three separate bandgap voltage reference circuits provide the voltage references V_{REF1} , V_{REF2} and V_{REF3}/V_{REF4} .

Power Supply level detection is provided by the Supply Detector circuit. The output of this circuit indicates whether the supply is above the threshold V_{SUPTH} .

There is an on-chip switch in series with the positive supply to the Bias circuit. The safety logic output "Drive Enable" closes or opens this switch to turn the Bias circuit on, or off, respectively.

FUNCTIONAL DESCRIPTION

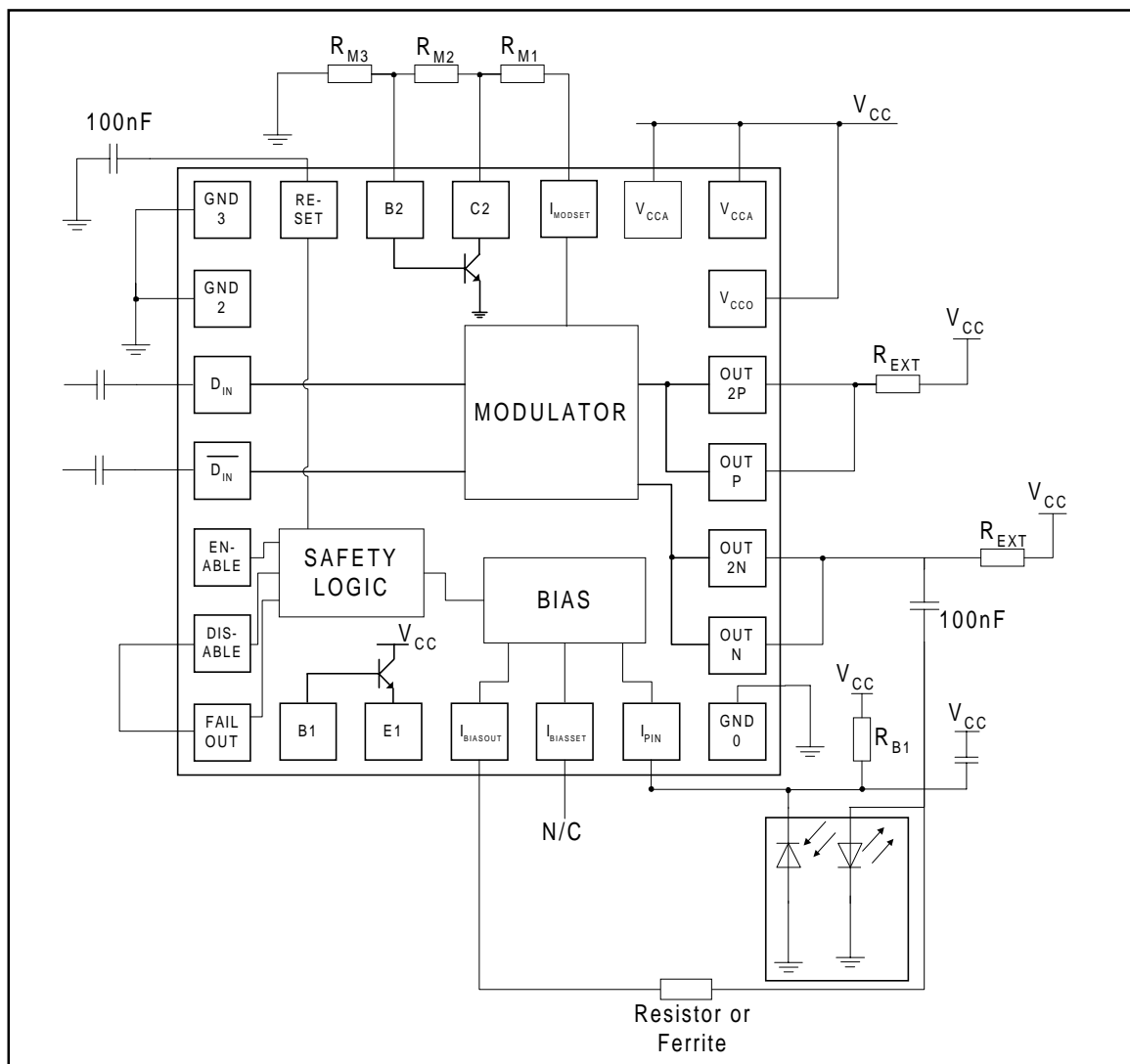


This diagram shows the detail of the Safety Logic. The bias circuit may be switched off using the ENABLE or DISABLE pin. It is also switched off if the supply is low.

If failure of the bias control circuit is detected, this condition is latched and indicated at the pin FAILOUT. The latch is RESET when the condition that ENABLE and SUPPLY OK are both true, is re-established. The length of the reset pulse is determined by the size of the external capacitor in combination with the internal 500kΩ resistor.

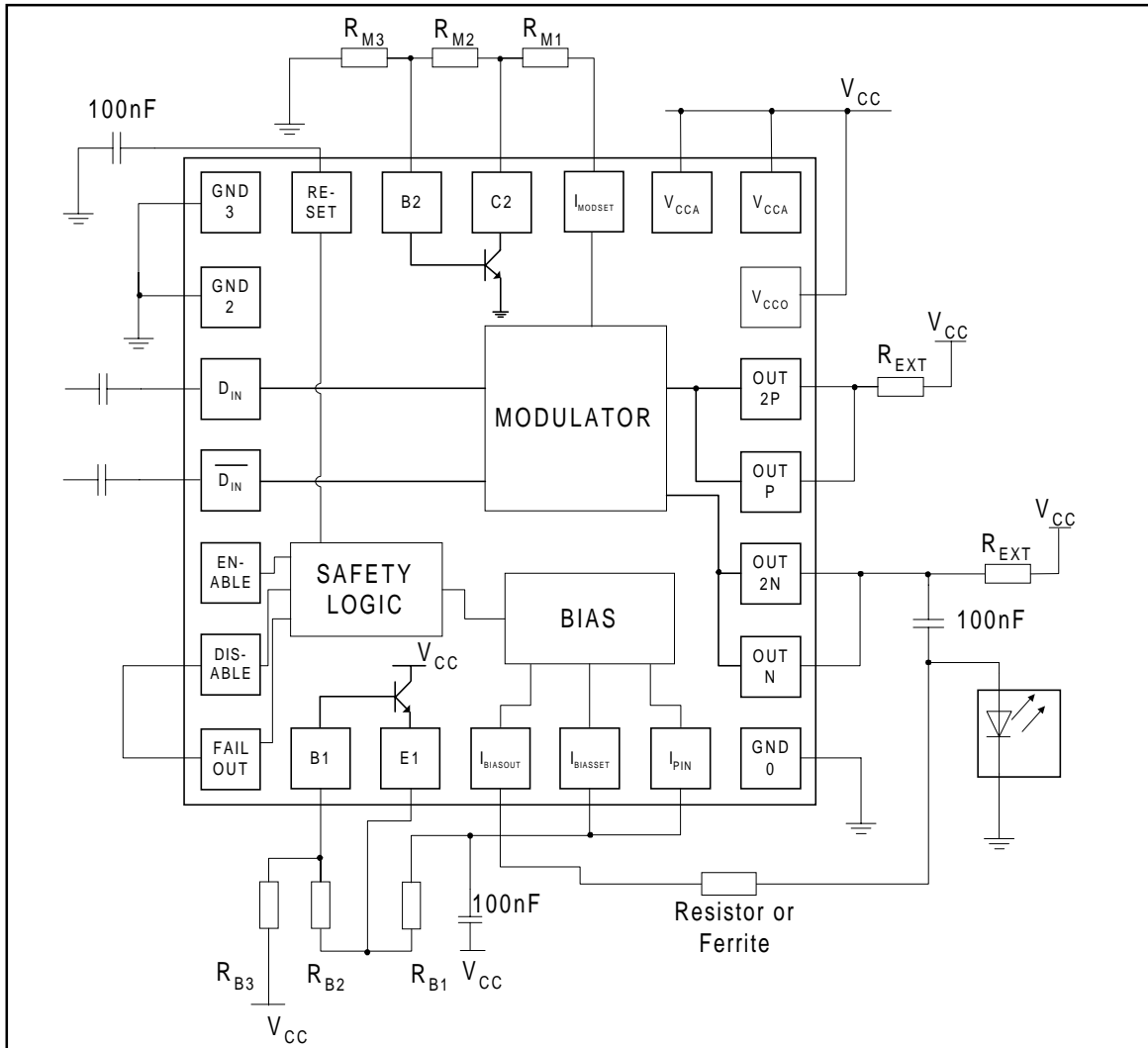
TYPICAL APPLICATIONS CIRCUIT

Closed Loop Operation



TYPICAL APPLICATIONS CIRCUIT

Open Loop Operation



DESIGN INFORMATION

Typical Closed Loop Application

Setting Bias Current for Closed Loop Operation

When the VCSEL includes a monitor photodiode, the closed loop scheme should be adopted. The voltage at I_{PIN} is equal to V_{CC}-1.2V, so the voltage across R_{B1} is 1.2V. The automatic power control loop increases or decreases I_{BIASOUT} such that the current from the monitor photodiode (and the VCSEL output power) remains constant. Knowing the monitor photodiode current (I_{PD}) at the desired output power, R_{B1} is set as follows:

$$R_{B1} = 1.2V / I_{PD}$$

Typical Open Loop Application

Setting Bias Current for Open Loop Operation:

When driving a device in open loop operation without a monitor photodiode, refer to the arrangement on page 9. The MC2062 can be configured to set VCSEL bias current with or without temperature compensation.

First calculate the nominal bias current:

$$I_{BIAS} = I_{TH} + \frac{P_{avg}}{\eta}$$

where I_{th} is the threshold current (in mA), P_{avg} is the average power (in mW), and η is the VCSEL slope efficiency (in mW/mA).

Next, the required temperature coefficient of bias current must be calculated. Note that with the modulation output AC coupled, the temperature coefficient of the VCSEL slope efficiency also affects the overall desired temperature coefficient of bias current:

$$TC_{BIAS} = \left(\frac{(TC_{ITH} \times I_{TH}) - \left(TC_{\eta} \times \frac{P_{avg}}{\eta} \right)}{I_{BIAS}} \right) - TC_{BIASOUT}$$

where TC_{ITH} is the temperature coefficient of threshold current (in ppm/°C), TC_η is the slope efficiency temperature coefficient (in ppm/°C), and TC_{BIASOUT} is

the temperature coefficient of I_{BIASOUT} with no programmed compensation – see DC Characteristics.

When not programming temperature compensation, the typical temperature coefficient of bias current is -1000ppm/°C. For this condition (no additional temperature compensation), connect R_{B1} between I_{PIN} and V_{CC} (R_{B2} and R_{B3} are not required). Knowing the desired VCSEL bias current, R_{B1} is calculated as follows:

$$R_{B1} = \frac{1.2V \times M_{IBIAS}}{I_{BIAS} \cdot C_{IBIAS}}$$

where M_{IBIAS} is a bias current multiplier and C_{IBIAS} is an offset – see DC Characteristics.

As noted, programming the bias current as listed above yields a temperature coefficient of -1000ppm/°C. By connecting pin B1 to V_{CC} and connecting R_{B1} between pin E1 and I_{PIN}, the bias current is typically ≈ 2000ppm/°C. With this configuration, R_{B1} is set as follows (R_{B2} and R_{B3} are not required):

$$R_{B1} = \frac{0.55V \times M_{IBIAS}}{I_{BIAS} \cdot C_{IBIAS}}$$

Finally, when more temperature compensation is required for I_{BIAS}, use the configuration as shown on page 9. The procedure for selecting the values for R_{B1}, R_{B2}, and R_{B3} is as follows:

1. Calculate the voltage at pin E1:

$$V_{E1} = \frac{TC_{IBIAS} \times 1.2V}{TC_{IBIAS} + 3000}$$

where V_{E1} is the number of volts below V_{CC}.

2. Calculate I(I_{BIASSET}):

$$I(I_{BIASSET}) = \frac{I_{BIAS} \cdot C_{IBIAS}}{M_{IBIAS}}$$

where M_{IBIAS} is the bias current multiplier and C_{IBIAS} is an offset – see DC Characteristics.

3. Calculate R_{B1}:

$$R_{B1} = \frac{1.2 - V_{E1}}{I(I_{BIASSET})}$$

4. Calculate the values for the temperature compen-

DESIGN INFORMATION

sation resistors, R_{B2} and R_{B3} :

$$R_{B2} = \frac{0.65V}{0.5 \times I(I_{BIASSET})}$$

$$R_{B3} = \frac{V_{E1} - 0.65V}{0.5 \times I(I_{BIASSET})}$$

The factor of 0.5 in the denominator of both equations sets the current through the temperature compensation transistor to half of $I_{BIASSET}$, allowing for adjustment of R_{B1} without impacting the temperature compensation.

Setting Modulation Current:

Refer to page 8 or 9. The modulation output current, I_{MOD} , from the Modulator is given by:

$$I_{MODOUT} = I(I_{MODSET}) \times M_{IMOD} + C_{IMOD}$$

Where $I(I_{MODSET})$ is the current output at pin I_{MODSET} , M_{IMOD} is a multiplier and C_{IMOD} is an offset current – see AC Characteristics. With the circuit configured as shown, the voltage at pin I_{MODSET} is equal to V_{REF1} .

First, calculate I_{MODOUT} :

$$I_{MODOUT} = \frac{I_{MODVCSEL} \times (R_{SER} + R_{SHUNT})}{R_{SHUNT}}$$

Where $R_{SHUNT} = R_{EXT} // 75\Omega$

Where $I_{MODVCSEL}$ is the modulation current required for the VCSEL itself, R_{SER} is the VCSEL series resistance, and R_{SHUNT} is the shunt pull-up resistance to V_{CC} . Keep in mind that any external value of pull-up resistance is in parallel with 75Ω internal on the MC2062.

From the previous equation,

$$I(I_{MODSET}) = \frac{I_{MODOUT} - C_{IMOD}}{M_{IMOD}}$$

Next, the required temperature coefficient of modulation current must be determined:

$$TC_{IMOD} = -TC_{\eta} - TC_{IOUT}$$

where TC_{IOUT} is the temperature coefficient of I_{MODOUT} with no programmed compensation – see AC Characteristics.

When not programming temperature compensation, the typical temperature coefficient of modulation current is $-250\text{ppm}/^{\circ}\text{C}$. For this condition (no additional temperature compensation), connect R_{M1} between I_{MODSET} and GND (R_{M2} and R_{M3} are not required). R_{M1} is calculated as follows:

$$R_{M1} = \frac{1.2V}{I(I_{MODSET})}$$

As noted, programming the modulation current as listed above yields a temperature coefficient of $-250\text{ppm}/^{\circ}\text{C}$. By connecting pin C2 to B2 and connecting R_{M1} between pin C2/B2 and I_{MODSET} , the temperature coefficient of modulation current is roughly $2750\text{ppm}/^{\circ}\text{C}$. With this configuration, R_{M1} is set as follows (R_{M2} and R_{M3} are not required):

$$R_{M1} = \frac{0.65V}{I(I_{MODSET})}$$

Finally, when more temperature compensation is required for I_{MODOUT} , use the configuration as shown on pages 8 and 9. The procedure for selecting the values for R_{M1} , R_{M2} , and R_{M3} is as follows:

1. Calculate the voltage at pin C2:

$$V_{C2} = \frac{TC_{IMOD} \times 1.2V}{TC_{IMOD} + 3000}$$

2. Calculate R_{M1} :

$$R_{M1} = \frac{1.2 - V_{C2}}{I(I_{MODSET})}$$

3. Calculate the values for the temperature compensation resistors, R_{M2} and R_{M3} :

$$R_{M2} = \frac{V_{C2} - 0.65V}{0.5 \times I(I_{MODSET})}$$

$$R_{M3} = \frac{0.65V}{0.5 \times I(I_{MODSET})}$$

The factor of 0.5 in the denominator of both equations sets the current through the temperature compensation transistor to half of $I(I_{MODSET})$, allowing for adjustment of R_{M1} without impacting the temperature compensation.

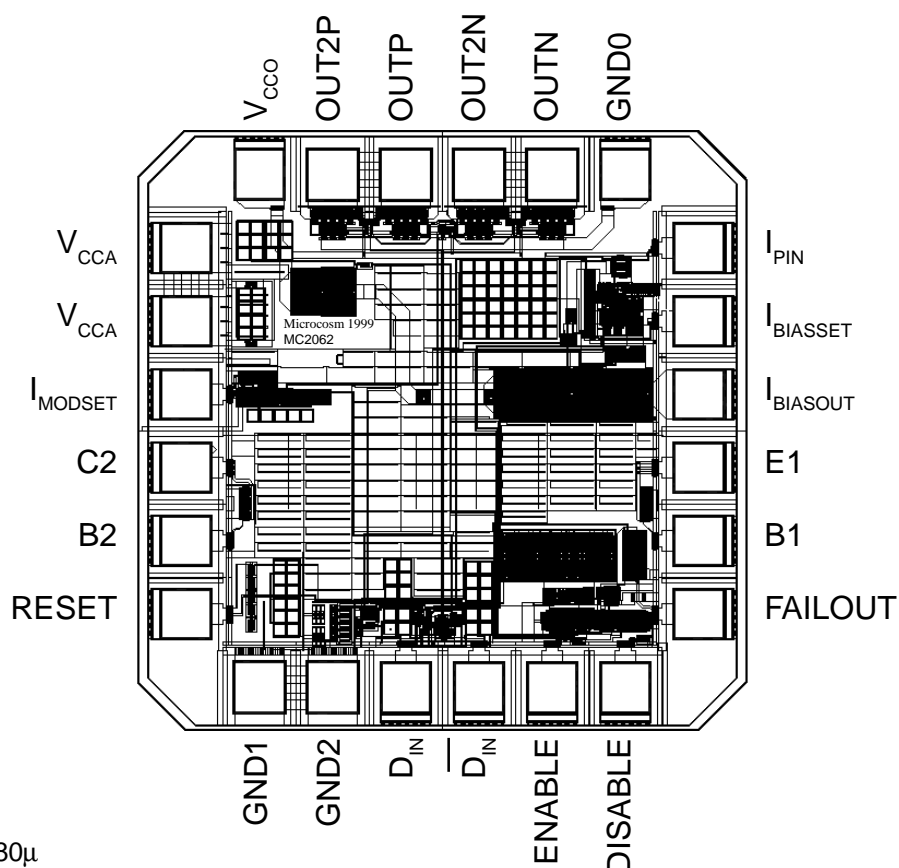
BARE DIE INFORMATION

Pad Centres

Description	X	Y
C2	-525	-75
B2	-525	-225
RESET	-525	-375
GND1	-375	-525
GND2	-225	-525
D _{IN}	-75	-525
\overline{D}_{IN}	75	-525
ENABLE	225	-525
DISABLE	375	-525
FAILOUT	525	-375
B1	525	-225
E1	525	-75

Description	X	Y
I _{BIASOUT}	525	75
I _{BIASSET}	525	225
I _{PIN}	525	375
GND0	375	525
OUTN	225	525
OUT2N	75	525
OUTP	-75	525
OUT2P	-225	525
V _{CCO}	-375	525
V _{CCA}	-525	375
V _{CCA}	-525	225
I _{MODSET}	-525	75

Chip Layout



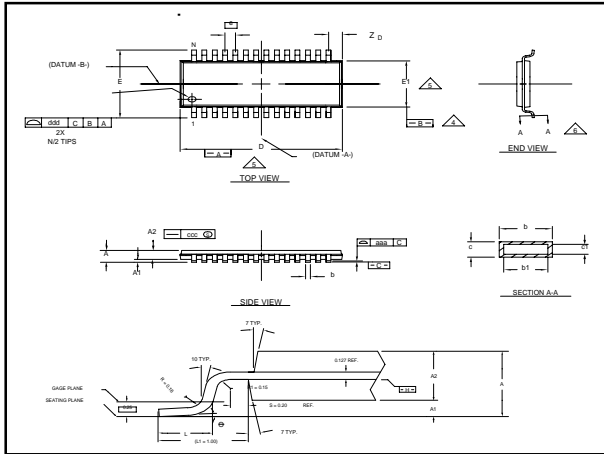
Dimensions:

Pad size 90x90 μ

Die Size 1280x1280 μ

PACKAGE INFORMATION

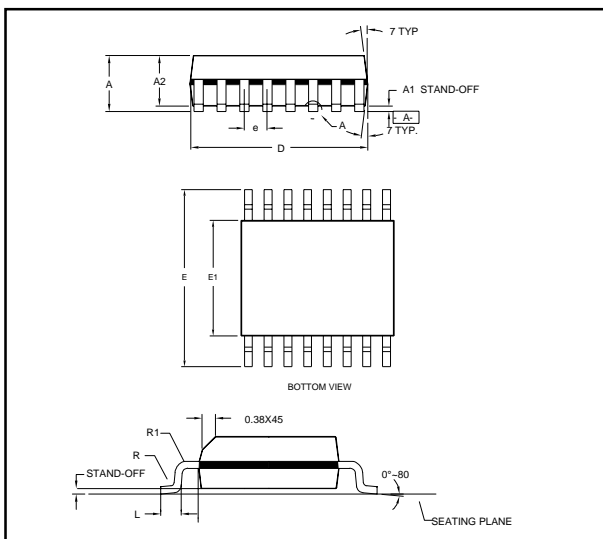
24 Lead Thin Small Shrink Outline Package (TSSOP)



Dims	Tols/Leads	20L	24L
A	MAX.	1.20	
A1		.05 MIN/.10 MAX	
A2	NOM.	.90	
D	± .05	6.50	7.80
E	± .10	6.40	
E1	± .10	4.40	
L	+ .15/- .10	.60	
L1	REF.	1.00	
Z _p	REF.	.325	

Dims	Tols/Leads	20L	24L
e	BASIC	.65	
b	± .05	.22	
c		.13 MIN/.20 MAX	
e	± 4°	4°	
aaa	MAX.	.10	
bbb	MAX.	.10	
ccc	MAX.	.05	
ddd	MAX.	.20	

16 Lead Quarter Small Outline Package (QSOP)



Dims	Tols/N	16
A	MAX.	1.60
A1	± .05	0.1
A2	± .10	1.40
D	± .10	4.9
E	± .20	6.00
E1	± .10	3.90
L	± .05	0.6

Dims	Tols/N	16
ccc	MAX.	0.10
ddd	MAX.	0.10
e	BASIC	0.65
b	± .05	0.25
c	± .05	.2 min .24 max
R	± .05	0.20
R1	MIN.	0.20

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