![Harris Semiconductor logo](Harris Semiconductor)

CD74LPT373

Fast CMOS 3.3V 8-Bit Transparent Latch

Features

- **Advanced 0.6 micron CMOS Technology**

- **Compatible with LCX™ Families of Products**
- **Supports 5V Tolerant Mixed Signal Mode Operation**
  - **Input Can Be 3V or 5V**
  - **Output Can Be 3V or Connected to 5V Bus**

- **Advanced Low Power CMOS Operation**

- **Excellent Output Drive Capability:**
  - **Balanced Drives (24mA Sink and Source)**

- **Low Ground Bounce Outputs**

- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE ($^\circ$C)	PACKAGE	PKG. NO.
CD74LPT373AM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT373AQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT373CM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT373CQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT373M	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT373QM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

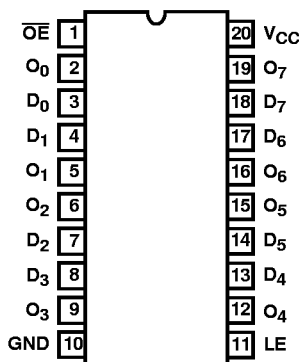When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

The CD74LPT373 is an 8-bit transparent latch designed with three-state outputs and is intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

The CD74LPT373 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.
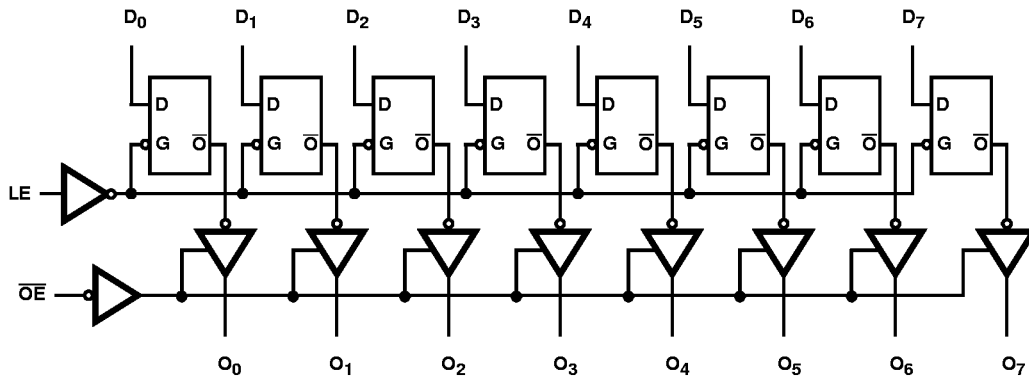
Pinout

CD74LPT373
(QSOP, SOIC)
TOP VIEW

```
        _____
 OE  [1]          [20] VCC
 O0  [2]          [19] O7
 D0  [3]          [18] D7
 D1  [4]          [17] D6
 O1  [5]          [16] O6
 O2  [6]          [15] O5
 D2  [7]          [14] D5
 D3  [8]          [13] D4
 O3  [9]          [12] O4
 GND [10]         [11] LE
        _____
```

File Number **4199.1**

CD74LPT373

Functional Block Diagram

TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
D_N	LE	$\overline{OE}$	O_N
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D_7-D_0	Data Inputs
O_7-O_0	Three-State Outputs
GND	Ground
V_{CC}	Power

CD74LPT373

Absolute Maximum Ratings

DC Input Voltage . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range. . . . . -40°C to 85°C
Supply Voltage to Ground Potential
    Inputs and V_{CC} Only . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
    Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (^{o}C/W)
    SOIC Package. 87
    QSOP Package 110
Maximum Junction Temperature . . . . .150°C
Maximum Storage Temperature Range . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s). . . . . .300°C
    (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	μA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	μA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	μA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	μA
High Impedance Output Current (Three-State)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	μA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	μA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

| PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq$ 4.5V		-	-	±100	μA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	μA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = VCC - 0.6V (Note 9)	-	2.0	30	μA
Dynamic Power Supply (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	μA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $\overline{OE}$ = GND 8 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT373		CD74LPT373A		CD74LPT373C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay D_X to O_X	t_{PLH}, t_{PHL}	$C_L = 50pF$ $R_L = 500\Omega$	1.5	8.0	1.5	5.2	1.5	4.2	ns
Propagation Delay LE to O_X	t_{PLH}, t_{PHL}		2.0	8.5	2.0	8.5	2.0	5.5	ns
Output Enable Time $\overline{OE}$ to O_X	t_{PZH}, t_{PZL}		1.5	8.5	1.5	6.5	1.5	5.5	ns
Output Disable Time (Note 16) $\overline{OE}$ to O_X	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.5	1.5	5.0	ns
Setup Time HIGH or LOW, D_X to LE	t_{SU}		2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, D_X to LE	t_H		1.5	-	1.5	-	1.5	-	ns
LE Pulse Width (Note 16) HIGH	t_W		6.0	-	5.0	-	5.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.

4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.

5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

6. This parameter is guaranteed but not tested.

7. $V_{OH} = V_{CC}$ - 0.6V at rated current.

8. This parameter is determined by device characterization but is not production tested.

9. Per TTL driven input; all other inputs at V_{CC} or GND.

10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.

13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

14. See test circuit and wave forms.

15. Minimum limits are guaranteed but not tested on Propagation Delays.

16. This parameter is guaranteed but not production tested.

17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms

PULSE GENERATOR V_{IN} **DUT** V_{OUT}

V_{CC}

6V
OPEN
GND
500Ω
R_T
50pF C_L
500Ω
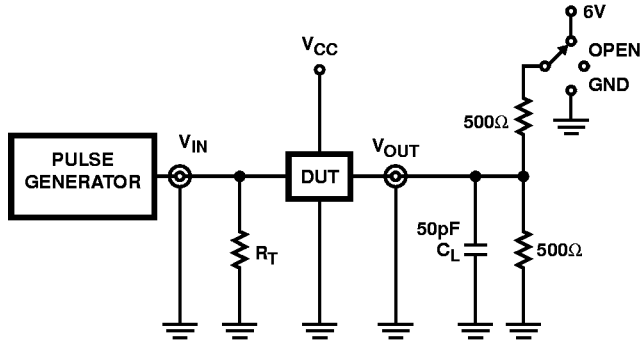
SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

DATA INPUT — 3V / 1.5V / 0V
t_{SU} t_H

TIMING INPUT — 3V / 1.5V / 0V

ASYNCHRONOUS CONTROL PRESET, CLEAR, ETC. — 3V / 1.5V / 0V
t_{REM}

SYNCHRONOUS CONTROL PRESET, CLEAR, CLOCK ENABLE, ETC. — 3V / 1.5V / 0V
t_{SU} t_H
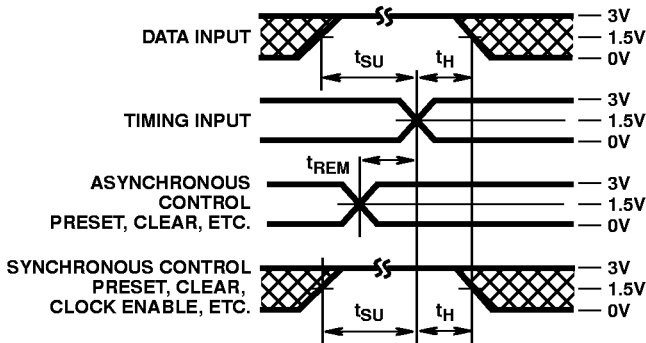
FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

LOW-HIGH-LOW PULSE — 1.5V
t_W

HIGH-LOW-HIGH PULSE — 1.5V

FIGURE 3. PULSE WIDTH

CONTROL INPUT
ENABLE DISABLE
3V / 1.5V / 0V

OUTPUT NORMALLY LOW
SWITCH 6V
3V / 1.5V
t_{PZL} t_{PLZ}
0.3V V_{OL}
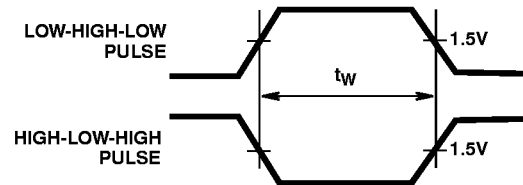
OUTPUT NORMALLY HIGH
SWITCH GND
1.5V / 0V
t_{PZH} t_{PHZ}
0.3V V_{OH}
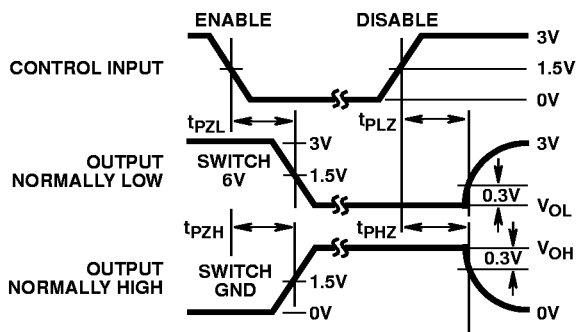
FIGURE 4. ENABLE AND DISABLE TIMING

SAME PHASE INPUT TRANSITION — 3V / 1.5V / 0V
t_{PLH} t_{PHL}

OUTPUT
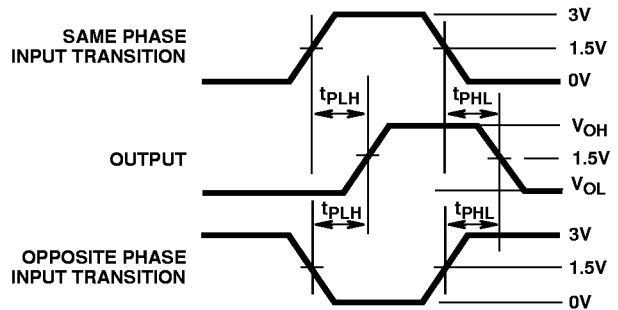V_{OH} / 1.5V / V_{OL}
t_{PLH} t_{PHL}

OPPOSITE PHASE INPUT TRANSITION — 3V / 1.5V / 0V

FIGURE 5. PROPAGATION DELAY