



# CY74FCT16652T CY74FCT162652T

## 16-Bit Registered Transceiver

### Features

- Low power, pin-compatible replacement for ABT functions
- FCT-E speed at 3.8 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to +85°C
- V<sub>CC</sub> = 5V ± 10%

#### CY74FCT16652T Features:

- 64 mA sink current, 32 mA source current
- Typical V<sub>OLP</sub> (ground bounce) < 1.0V at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C

#### CY74FCT162652T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical V<sub>OLP</sub> (ground bounce) < 0.6V at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C

### Functional Description

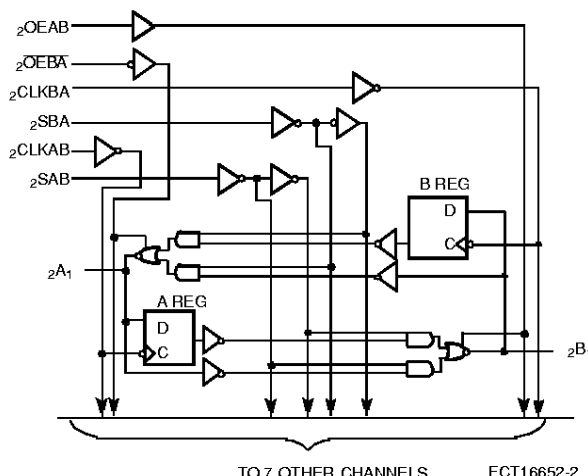
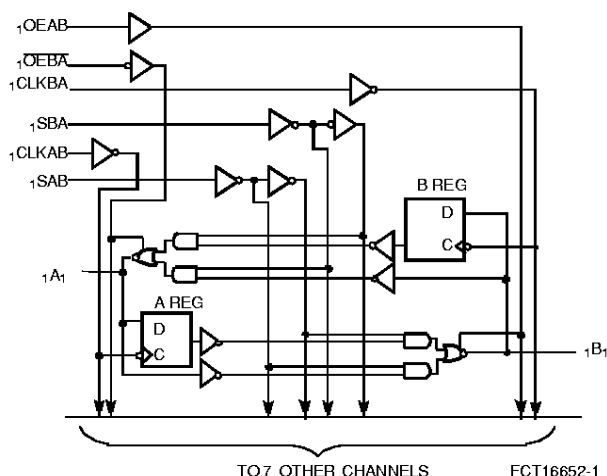
These 16-bit, high-speed, low-power, registered transceivers that are organized as two independent 8-bit bus transceivers with three-state D-type registers and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. OEAB and OEBA control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CLKAB or CLKBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state. The output buffers are designed with a power-off disable feature that allows live insertion of boards.

The CY74FCT16652T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162652T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162652T is ideal for driving transmission lines.

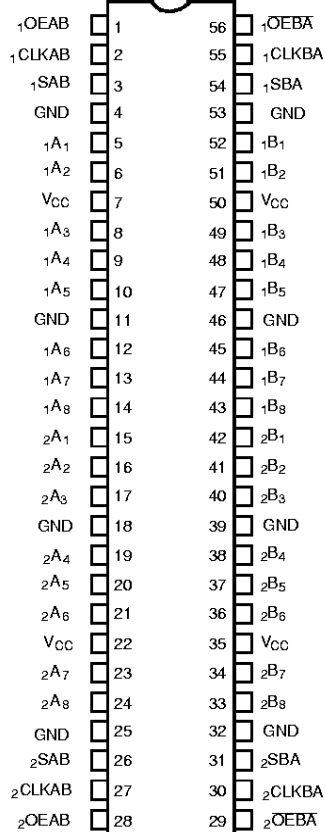
### Logic Block Diagrams



### Pin Configuration

SSOP/TSSOP

Top View



FCT16652-3

### Pin Description

Name	Description
A	Data Register A Inputs Data Register B Outputs
B	Data Register B Inputs Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

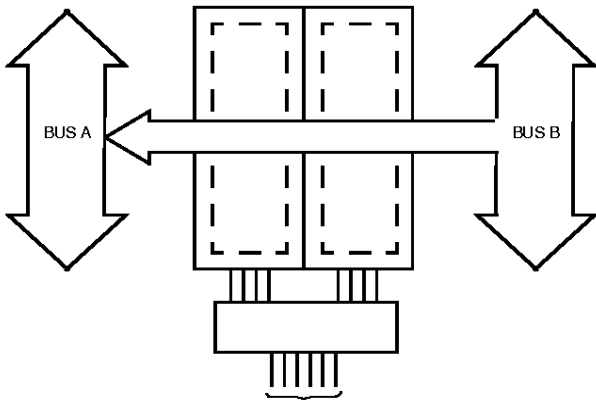


**Function Table<sup>[1]</sup>**

Inputs						Data I/O <sup>[2]</sup>		Operation or Function
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A	B	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	┐	┐	X	X			Store A and B Data
X	H	┐	H or L	X	X	Input	Unspecified <sup>[2]</sup>	Store A, Hold B
H	H	┐	┐	X <sup>[3]</sup>	X	Input	Output	Store A in Both Registers
L	X	H or L	┐	X	X	Unspecified <sup>[2]</sup>	Input	Hold A, Store B
L	L	┐	┐	X	X <sup>[3]</sup>		Input	Store B in both Registers
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

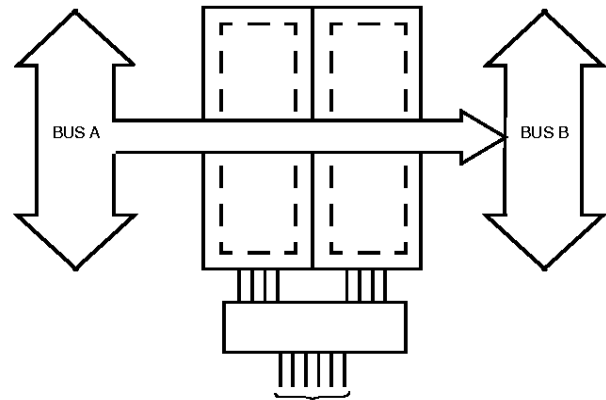
**Notes:**

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
┐ = LOW-to-HIGH Transition
- The data output functions may be enabled or disabled by various signals at the OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- Select control=L; clocks can occur simultaneously.  
Select control=H; clocks must be staggered to load both registers.



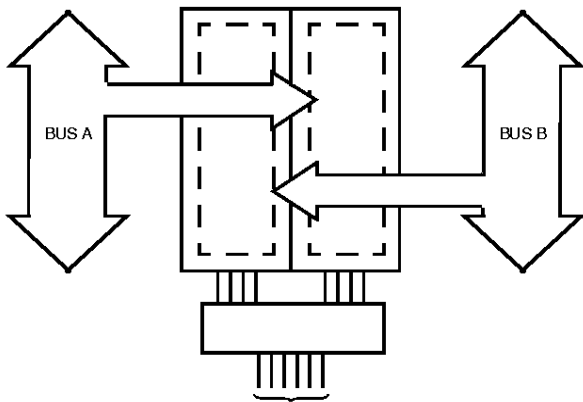
OEAB L    OEBA L    CLKAB X    CLKBA X    SAB X    SBA L

Real-Time Transfer  
Bus B to Bus A



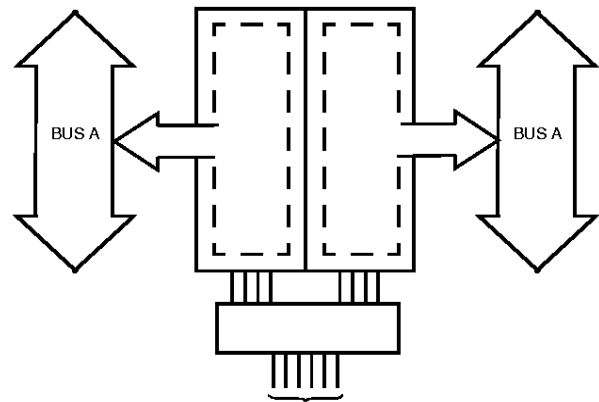
OEAB H    OEBA L    CLKAB X    CLKBA X    SAB L    SBA X

Real-Time Transfer  
Bus A to Bus B



OEAB X    OEBA H    CLKAB X    CLKBA X    SAB X    SBA X  
 L    L    L    L    X    X  
 L    H    X    X

Storage from  
A and/or B



OEAB H    OEBA L    CLKAB H or L    CLKBA H or L    SAB H    SBA H

Transfer Stored Data  
to A and/or B

### Maximum Ratings<sup>[4]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	Com'l	-55°C to +125°C
Ambient Temperature with Power Applied .....	Com'l	-55°C to +125°C
DC Input Voltage .....		-0.5V to +7.0V
DC Output Voltage .....		-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin) .....		-60 to +120 mA

**Note:**

- Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Dissipation .....	1.0W
Static Discharge Voltage .....	>2001V (per MIL-STD-883, Method 3015)

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	5V ± 10%



**DC Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions <sup>[5]</sup>	Min.	Typ. <sup>[6]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
V <sub>H</sub>	Input Hysteresis			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>			±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>I</sub> =GND			±1	μA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V			±1	μA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V			±1	μA
I <sub>OS</sub>	Short Circuit Current <sup>[8]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[8]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V	-50		-180	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V <sup>[7]</sup>			±1	μA

**Output Drive Characteristics for CY74FCT16652T**

Parameter	Description	Test Conditions <sup>[5]</sup>	Min.	Typ. <sup>[6]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-3 mA	2.5	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	2.4	3.5		
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	2.0	3.0		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.2	0.55	V

**Output Drive Characteristics for CY74FCT162652T**

Parameter	Description	Test Conditions <sup>[5]</sup>	Min.	Typ. <sup>[6]</sup>	Max.	Unit
I <sub>ODL</sub>	Output LOW Current <sup>[8]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	60	115	150	mA
I <sub>ODH</sub>	Output HIGH Current <sup>[8]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	-60	-115	-150	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-24 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =24 mA		0.3	0.55	V

**Capacitance** (T<sub>A</sub> = +25°C, f = 1.0 MHz)

Parameter	Description <sup>[10]</sup>	Test Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8.0	pF

**Notes:**

5. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
6. Typical values are at V<sub>CC</sub>=5.0V, +25°C ambient.
7. Tested at T<sub>A</sub>= +25°C.
8. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
9. Duration of the condition cannot exceed one second.
10. This parameter is measured at characterization but not tested.



### Power Supply Characteristics

Param.	Description	Test Conditions <sup>[11]</sup>		Min.	Typ. <sup>[12]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$	—	5	500	$\mu A$
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = 3.4V$ <sup>[13]</sup>	—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>[14]</sup>	$V_{CC} = \text{Max.}$ Outputs Open OEAB=OEBA=GND One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	—	75	120	$\mu A / \text{MHz}$
$I_C$	Total Power Supply Current <sup>[15]</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_o = 10 \text{ MHz (CLKBA)}$ 50% Duty Cycle OEAB=OEBA=GND One-Bit Toggling $f_1 = 5 \text{ MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	—	1.3	3.2	mA
		$V_{CC} = \text{Max.}$ Outputs Open $f_o = 10 \text{ MHz (CLKBA)}$ 50% Duty Cycle OEAB=OEBA=GND Sixteen Bits Toggling $f_1 = 2.5 \text{ MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	—	3.8	6.5 <sup>[16]</sup>	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	—	8.3	20.0 <sup>[16]</sup>	mA

**Notes:**

11. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
12. Typical values are at  $V_{CC} = 5.0V$  +25° ambient.
13. Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
14. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
15.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_o$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
16. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.



**Switching Characteristics** Over the Operating Range<sup>[17]</sup>

Parameter	Description	CY74FCT16652T CY74FCT162652T		CY74FCT16652AT CY74FCT162652AT		Unit	Fig. No. <sup>[18]</sup>
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Bus to Bus	1.5	9.0	1.5	6.3	ns	1, 3
t <sub>PZH</sub> t <sub>PHL</sub>	Output Enable Time OEAB or OEBA to Bus	1.5	14.0	1.5	9.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEAB or OEBA to Bus	1.5	9.0	1.5	6.3	ns	1, 7, 8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Bus	1.5	9.0	1.5	6.3	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SBA or SAB to Bus	1.5	11.0	1.5	7.7	ns	1, 5
t <sub>SU</sub>	Set-Up time HIGH or LOW Bus to Clock	2.0	—	2.0	—	ns	4
t <sub>H</sub>	Hold Time HIGH or LOW Bus to Clock	1.5	—	1.5	—	ns	4
t <sub>w</sub>	Clock Pulse Width HIGH or LOW	5.0	—	5.0	—	ns	5
t <sub>SK(O)</sub>	Output Skew <sup>[19]</sup>	—	0.5	—	0.5	ns	

Parameter	Description	CY74FCT16652CT CY74FCT162652CT		CY74FCT16652ET CY74FCT162652ET		Unit	Fig. No. <sup>[18]</sup>
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Bus to Bus	1.5	5.4	1.5	3.8	ns	1, 3
t <sub>PZH</sub> t <sub>PHL</sub>	Output Enable Time OEAB or OEBA to Bus	1.5	7.8	1.5	4.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEAB or OEBA to Bus	1.5	6.3	1.5	4.0	ns	1, 7, 8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Bus	1.5	5.7	1.5	3.8	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SBA or SAB to Bus	1.5	6.2	1.5	4.2	ns	1, 5
t <sub>SU</sub>	Set-Up Time HIGH or LOW Bus to Clock	2.0	—	2.0	—	ns	4
t <sub>H</sub>	Hold Time HIGH or LOW Bus to Clock	1.5	—	0.0	—	ns	4
t <sub>w</sub>	Clock Pulse Width HIGH or LOW	5.0	—	3.0	—	ns	5
t <sub>SK(O)</sub>	Output Skew <sup>[19]</sup>	—	0.5	—	0.5	ns	

**Notes:**

17. Minimum limits are guaranteed, but not tested, on propagation delays.

18. See "Parameter Measurement Information" in the General Information section.

19. Skew between any two outputs of the same package switching in the same direction. This parameter guaranteed by design.



**Ordering Information CY74FCT16652**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT16652ETPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16652ETPVC	O56	56-Lead (300-Mil) SSOP	
5.4	CY74FCT16652CTPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16652CTPVC	O56	56-Lead (300-Mil) SSOP	
6.3	CY74FCT16652ATPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16652ATPVC	O56	56-Lead (300-Mil) SSOP	
9.0	CY74FCT16652TPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16652TPVC	O56	56-Lead (300-Mil) SSOP	

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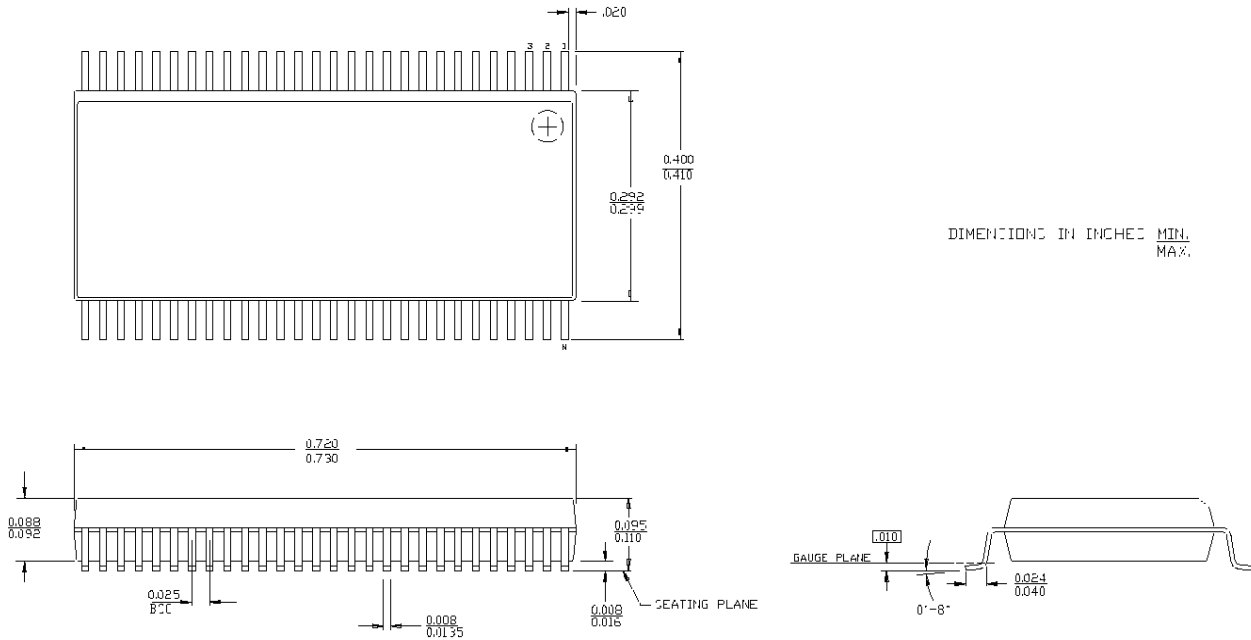
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT162652ETPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162652ETPVC	O56	56-Lead (300-Mil) SSOP	
5.4	CY74FCT162652CTPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162652CTPVC	O56	56-Lead (300-Mil) SSOP	
6.3	CY74FCT162652ATPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162652ATPVC	O56	56-Lead (300-Mil) SSOP	
9.0	CY74FCT162652TPAC	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162652TPVC	O56	56-Lead (300-Mil) SSOP	

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**Package Diagrams**

**56-Lead Shrunken Small Outline Package O56**



**56-Lead Thin Shrunken Small Outline Package Z56**

