

# UT54ACS00/UT54ACTS00

Radiation-Hardened  
Quadruple 2-Input NAND Gates

## FEATURES

- 1.2μ radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 14-pin DIP
  - 14-lead flatpack

## DESCRIPTION

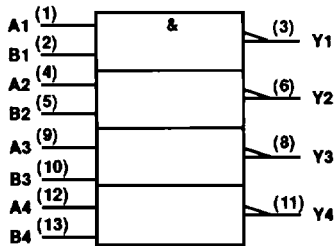
The UT54ACS00 and the UT54ACTS00 are quadruple, two-input NAND gates. The circuits perform the Boolean functions  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

The devices are characterized over full military temperature range of -55°C to +125°C.

## FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

## LOGIC SYMBOL

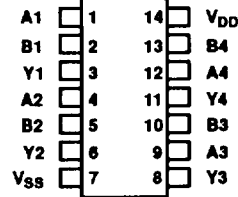


### Note:

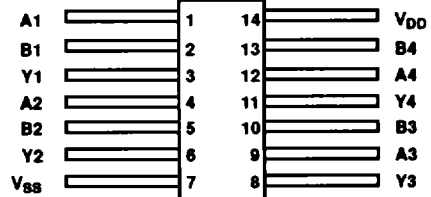
1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

## PINOUTS

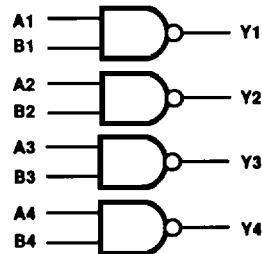
### 14-Pin DIP Top View



### 14-Lead Flatpack Top View



## LOGIC DIAGRAM



## RADIATION HARDNESS SPECIFICATIONS <sup>1</sup>

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU & SEL Threshold <sup>2</sup>	80	MeV-cm <sup>2</sup> /mg
Neutron Fluence	1.0E14	n/cm <sup>2</sup>

**Notes:**

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD</sub>	Supply voltage	-0.3 to 7.0	V
V <sub>I/O</sub>	Voltage any pin	-.3 to V <sub>DD</sub> +.3	V
T <sub>STG</sub>	Storage Temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+175	°C
T <sub>LS</sub>	Lead temperature (soldering 5 seconds)	+300	°C
θ <sub>JC</sub>	Thermal resistance junction to case	20	°C/W
I <sub>I</sub>	DC input current	± 10	mA
P <sub>D</sub>	Maximum power dissipation	1	W

**Note:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD</sub>	Supply voltage	4.5 to 5.5	V
V <sub>IN</sub>	Input voltage any pin	0 to V <sub>DD</sub>	V
T <sub>C</sub>	Temperature range	-55 to +125	°C

## DC ELECTRICAL CHARACTERISTICS <sup>7</sup>

( $V_{DD} = 5.0V \pm 10\%$ ;  $V_{SS} = 0V$ <sup>6</sup>;  $-55^{\circ}C < T_C < +125^{\circ}C$ )

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
$V_{IL}$	Low-level input voltage <sup>1</sup> ACTS ACS			0.8 .3 $V_{DD}$	V
$V_{IH}$	High-level input voltage <sup>1</sup> ACTS ACS		.5 $V_{DD}$ .7 $V_{DD}$		V
$I_{IN}$	Input leakage current ACTS/ACT	$V_{IN} = V_{DD}$ or $V_{SS}$	-1	1	$\mu A$
$V_{OL}$	Low-level output voltage <sup>3</sup> ACTS ACS	$I_{OL} = 8.0mA$ $I_{OL} = 100\mu A$		0.40 0.25	V
$V_{OH}$	High-level output voltage <sup>3</sup> ACTS ACS	$I_{OH} = -8.0mA$ $I_{OH} = -100\mu A$	.7 $V_{DD}$ $V_{DD} - 0.25$		V
$I_{OS}$	Short-circuit output current <sup>2,4</sup> ACTS/ACS	$V_O = V_{DD}$ and $V_{SS}$	-200	200	mA
$P_{total}$	Power dissipation <sup>8,9</sup>	$C_L = 50pF$		1.8	mW/MHz
$I_{DDQ}$	Quiescent Supply Current	$V_{DD} = 5.5V$		100	$\mu A$
$C_{IN}$	Input capacitance <sup>5</sup>	$f = 1MHz @ 0V$		15	pF
$C_{OUT}$	Output capacitance <sup>5</sup>	$f = 1MHz @ 0V$		15	pF

### Notes:

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH}(\min) + 20\%$ ,  $-0\%$ ;  $V_{IL} = V_{IL}(\max) + 0\%$ ,  $-50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH}(\min)$  and  $V_{IL}(\max)$ .
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-M-38510, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose  $\leq 1E6$  rads(Si).
- Power does not include power contribution of any TTL output sink current.
- Power dissipation specified per switching output.

## AC ELECTRICAL CHARACTERISTICS <sup>2</sup>

( $V_{DD} = 5.0V \pm 10\%$ ;  $V_{SS} = 0V$ <sup>1</sup>;  $-55^{\circ}C < T_C < +125^{\circ}C$ )

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
$t_{PHL}$	Input to Yn	1	14	ns
$t_{PLH}$	Input to Yn	1	11	ns

### Notes:

- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose  $\leq 1E6$  rads(Si).