

Triple three-input NAND ('F10) / AND ('F11) gates

54F10/54F11

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
14-Pin Ceramic DIP	54F10/BCA, 54F11/BCA	GDIP1-T14
14-Pin Ceramic Flat Pack	54F10/BDA, 54F11/BDA	GDFP1-F14
20-Pin Ceramic LLCC	54F10/B2A, 54F11/B2A	CQCC2-N20

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Y('F10)	Y('F11)
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = High voltage level
L = Low voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A - C	Inputs	1.0/1.0	20µA/0.6mA
Y, Ȳ	Output	50/33	1.0mA/20mA

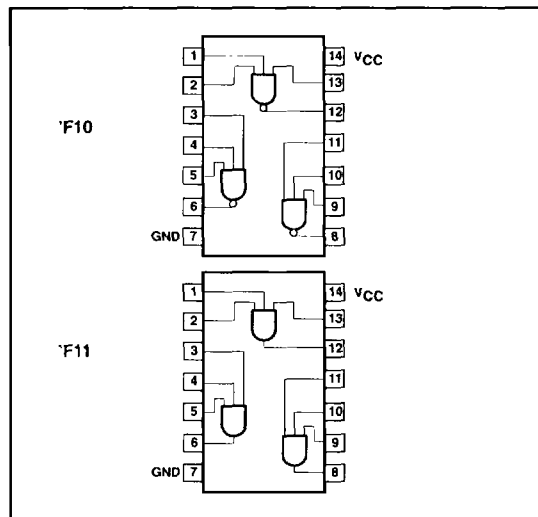
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

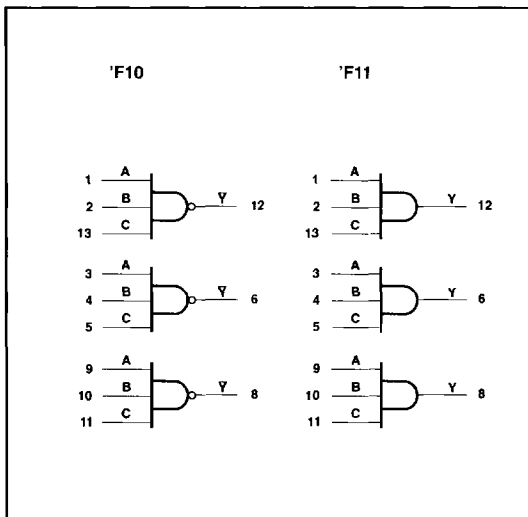
(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage range	-0.5 to +7.0	V
V _I	Input voltage range	-0.5 to +7.0	V
I _I	Input current range	-30 to +5	mA
V _O	Voltage applied to output in High output state range	-0.5 to +V _{CC}	V
I _O	Current applied to output in Low output state	40	mA
T _{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



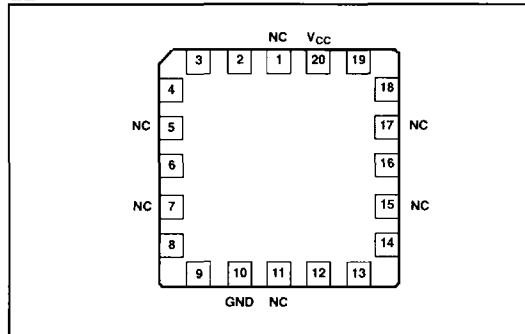
LOGIC SYMBOL



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LLCC LEAD CONFIGURATION



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT		
			MIN	TYP ²	MAX			
V_{OH}	High-level output voltage	$V_{CC} = \text{Min}, V_{IL} = \text{Max}, I_{OH} = \text{Max}, V_{IH} = \text{Min}$	2.5			V		
V_{OL}	Low-level output voltage	$V_{CC} = \text{Min}, V_{IL} = \text{Max}, I_{OL} = \text{Max}, V_{IH} = \text{Min}$		0.35	0.50	V		
V_{IK}	Input clamp voltage	$V_{CC} = \text{Min}, I_I = I_{IK}$		-0.73	-1.2	V		
I_{IH2}	Input current at maximum input voltage	$V_{CC} = \text{Max}, V_I = 7.0\text{V}$			100	μA		
I_{IH1}	High-level input current	$V_{CC} = \text{Max}, V_I = 2.7\text{V}$		1	20	μA		
I_{IL}	Low-level input current	$V_{CC} = \text{Max}, V_I = 0.5\text{V}$		-0.4	-0.6	mA		
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{Max}, V_O = 0.0\text{V}$	-60	-75	-150	mA		
I_{CC}	Supply current (total)	'F10	I_{CCH}	$V_{CC} = \text{Max}$	$V_I = \text{GND}$	1.8	2.1	mA
			I_{CCL}		$V_I \geq 4.0\text{V}$	6.0	7.7	mA
		'F11	I_{CCH}		$V_I \geq 4.0\text{V}$	4.7	6.2	mA
			I_{CCL}		$V_I = \text{GND}$	7.2	9.7	mA

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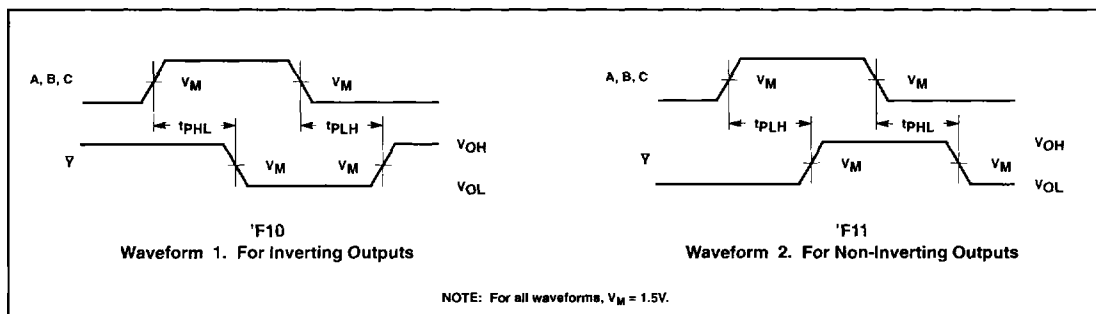
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _A = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _A = -55°C to +125°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay A, B, C to Y	Waveform 1 'F10	2.4 2.0	3.7 3.2	5.0 4.3	2.0 1.5	7.0 6.5	ns ns
t _{PLH} t _{PHL}	Propagation delay A, B, C to Y	Waveform 2 'F11	3.0 2.5	4.2 4.1	5.6 5.5	2.5 2.0	7.5 7.5	ns ns

NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC WAVEFORMS



TEST CIRCUIT AND WAVEFORM

