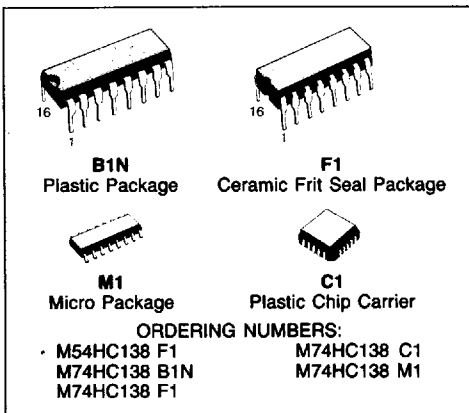


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T-67-21-55

3 TO 8 LINE DECODER (INVERTING)

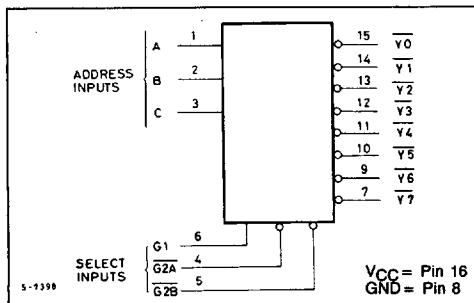
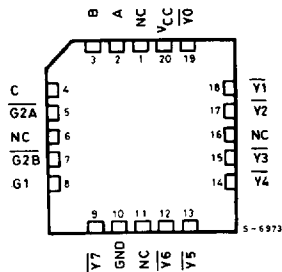
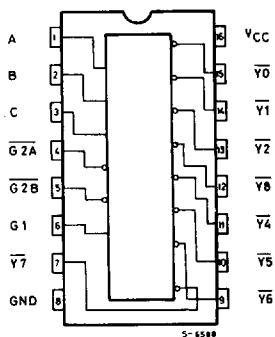
- HIGH SPEED
 $t_{pD} = 17ns$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu A$ at $T_A = 25^\circ C$
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = |I_{OL}|$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- WIDE OPERATING VOLTAGE RANGE
 V_{CC} (OPR) = 2 to 6V
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS138

**DESCRIPTION**

The M54/74HC138 is a high speed CMOS 3 TO 8 LINE DECODER fabricated in silicon gate C²MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. If the device is enabled, 3 binary select inputs (A, B and C) determine which one of the outputs will go low. If enable input G1 is held low or either G2A or G2B is held high, the decoding function is inhibited and all the 8 outputs go high.

Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

BLOCK DIAGRAM**PIN CONNECTIONS (top view)**

NC =
No Internal
Connection

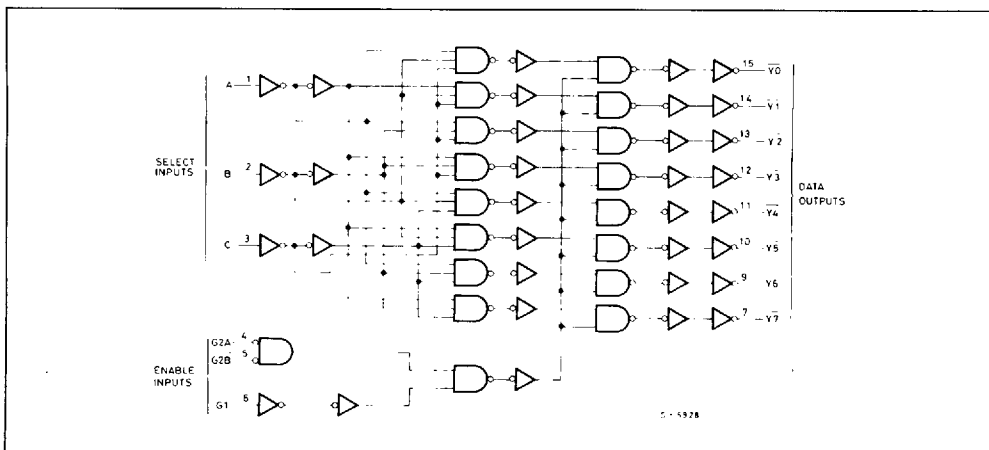
TRUTH TABLE

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INPUTS						OUTPUTS							SELECTED OUTPUT	
ENABLE			SELECT			$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$		$\overline{Y_7}$
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A									
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y_0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y_1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y_2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y_3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y_4}$
H	L	L	H	L	H	H	H	H	H	L	H	H	H	$\overline{Y_5}$
H	L	L	H	H	L	H	H	H	H	H	L	H	H	$\overline{Y_6}$
H	L	L	H	H	H	H	H	H	H	H	H	L	H	$\overline{Y_7}$

X: DON'T CARE

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	DC Input Voltage	0 to V_{CC}	V	
V_O	DC Output Voltage	0 to V_{CC}	V	
T_A	Operating Temperature	74HC Series 54HC Series	-55 to 125 -40 to 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} { 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to 7	V
V _I	DC Input Voltage	-0.5 to V _{CC} +0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} +0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW = derate to 10 mW/°C from 65°C to 85°C for plastic package

(*) 500 mW = derate to 12 mW/°C from 100 to 125°C for frit-seal package

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0		1.5	—	—	1.5	—	1.5	—	V	
		4.5		3.15	—	—	3.15	—	3.15	—		
		6.0		4.2	—	—	4.2	—	4.2	—		
V _{IL}	Low Level Input Voltage	2.0		—	—	0.5	—	0.5	—	0.5	V	
		4.5		—	—	1.35	—	1.35	—	1.35		
		6.0		—	—	1.8	—	1.8	—	1.8		
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	4.4	—	
		6.0	5.9	6.0	—	5.9	—	5.9	—	—		
		4.5	V _{IH} or V _{IL}	I _O	4.18	4.31	—	4.13	—	4.10	—	
6.0	5.68	5.8			—	5.63	—	5.60	—			
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0	—	0.0	0.1	—	0.1	—	0.1			
		4.5	V _{IH} or V _{IL}	I _O	4.0	0.17	0.26	—	0.33	—	0.40	
6.0	5.2	0.18			0.26	—	0.33	—	0.40			
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND	—	—	±0.1	—	±1.0	—	±1.0	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND	—	—	4	—	40	—	80	μA	

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $T_A=25^\circ C$, $C_L=15pF$, Input $t_r=t_f=6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C-Y)		17	27	ns
t_{PHL}	Propagation Delay Time (G, \bar{G} -Y)		15	23	ns

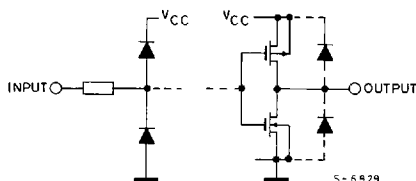
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AC ELECTRICAL CHARACTERISTICS ($C_L=50pF$, Input $t_r=t_f=6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ C$ 54HC and 74HC			-40 to $85^\circ C$ 74HC		-55 to $125^\circ C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
				t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	
t_{PLH} t_{PHL}	Propagation Delay Time (A,B,C- \bar{Y})	2.0 4.5 6.0		— — —	84 21 18	165 33 28	— — —	205 41 35	— — —	250 50 43	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G, \bar{G} -Y)	2.0 4.5 6.0		— — —	72 18 15	145 29 25	— — —	180 36 31	— — —	220 44 37	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	57	—	—	—	—	—	pF

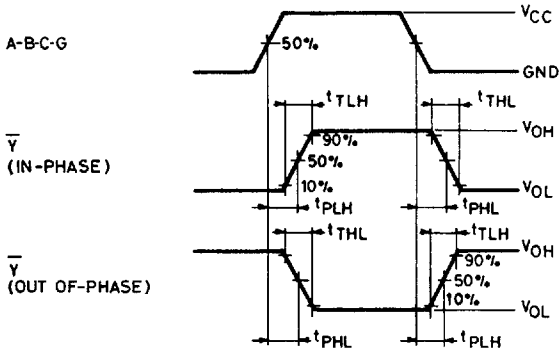
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

$$\text{Average operating current is: } I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

INPUT AND OUTPUT EQUIVALENT CIRCUIT

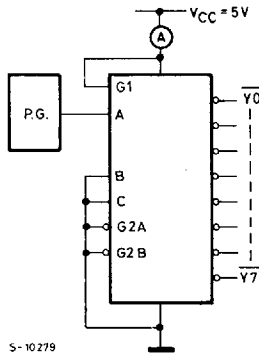
SWITCHING CHARACTERISTICS TEST WAVEFORM

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S-10278

TEST CIRCUIT I_{CC} (Opr.)



S-10279

INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.