4543B

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER FOR LIQUID CRYSTALS

DESCRIPTION – The 4543B is a BCD to 7-Segment Latch/Decoder/Driver for Liquid Crystal Displays with four Address Inputs (A_0-A_3), a Latch Enable Input (EL), a Blanking Input (I_B), a Clock Control Input (CP), and seven Segment Outputs (a-g).

When the Latch Enable Input (EL) is HIGH, the state of the Segment Outputs (a-g) is determined by the data on the four Address Inputs (A_0-A_3) and the Clock Control Input (CP). For driving Liquid Crystal Displays, a square wave must be applied to the CP input and to the electrically common backplane of the display. For common Cathode LED displays a LOW logic level must be applied to the CP input. For common anode LED displays a HIGH logic level must be applied to the CP input. When the Latch Enable Input (EL) goes LOW, the last data present at the address Inputs (A_0-A_3) is stored in the latches and the Segment Outputs (a-g) remain stable.

A HIGH on the Blanking Input (I_B) forces all Segment Outputs (a-g) LOW. The Blanking Input (I_B) does not affect the latch circuit.

- **BLANKING INPUT**
- **MULTIPLEXING CAPABILITY**
- **LCD DISPLAY OR COMMON ANODE OR COMMON CATHODE LED DISPLAY CAPABILITY**
- **BLANKING ON ALL ILLEGAL INPUT COMBINATIONS**

PIN NAMES

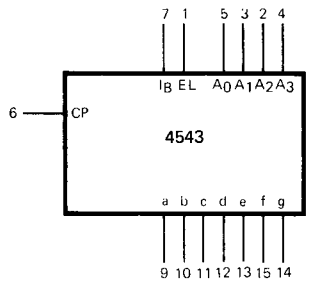
A_0-A_3	Address (Data) Inputs
EL	Latch Enable Input
I_B	Blanking Input
CP	Clock Control Input
a-g	Segment Outputs

TRUTH TABLE

INPUTS							OUTPUTS							
CP*	EL	I_B	A_3	A_2	A_1	A_0	a	b	c	d	e	f	g	DISPLAY
L	X	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	L	L	L	L	L	H	H	H	H	H	H	L	0
L	H	L	L	L	L	H	L	H	H	L	L	L	L	1
L	H	L	L	L	H	L	H	H	L	H	H	L	H	2
L	H	L	L	L	H	H	H	H	H	H	L	L	H	3
L	H	L	L	H	L	L	L	H	H	L	L	H	H	4
L	H	L	L	H	L	H	H	L	H	H	L	H	H	5
L	H	L	L	H	H	L	H	L	H	H	H	H	H	6
L	H	L	L	H	H	H	H	H	H	L	L	L	L	7
L	H	L	H	L	L	L	H	H	H	H	H	H	H	8
L	H	L	H	L	L	H	H	H	H	H	L	H	H	9
L	H	L	H	L	H	L	L	L	L	L	L	L	L	BLANK
L	H	L	H	L	H	H	L	L	L	L	L	L	L	BLANK
L	H	L	H	H	L	L	L	L	L	L	L	L	L	BLANK
L	H	L	H	H	L	H	L	L	L	L	L	L	L	BLANK
L	H	L	H	H	H	L	L	L	L	L	L	L	L	BLANK
L	H	L	H	H	H	H	L	L	L	L	L	L	L	BLANK
L	L	L	X	X	X	X	**							**
H	***	***	***				Inverse of the above Output Combinations							Display as Above

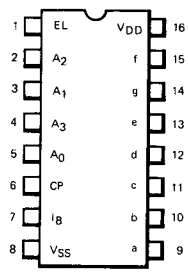
H = HIGH Level
L = LOW Level
X = Don't Care
* = For Liquid Crystal displays a square wave is applied to CP. For common cathod Light Emitting Diode displays a LOW logic level is applied to CP. For common anode Light Emitting Diode displays a HIGH logic level is applied to CP.
** = Depends upon the BCD Code applied during the HIGH-to-LOW transition of EL.
*** = The above combinations of logic levels.

LOGIC SYMBOL



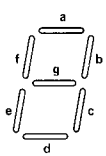
V_{DD} = PIN 16
V_{SS} = PIN 8

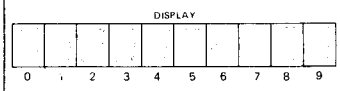
CONNECTION DIAGRAM DIP (TOP VIEW)



Note: The flatpack version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

NUMERICAL DESIGNATIONS





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