011559 011541

Am54/74174 • Am54/74175

Hex/Quadruple D-Type Flip-Flops with Clear

Distinctive Characteristics

- Buffered clock and direct clear inputs.
- Individual data input to each flip-flop.
- 35 MHz typical clock frequency.
- 100% reliability assurance testing in compliance with MIL-STD-883.

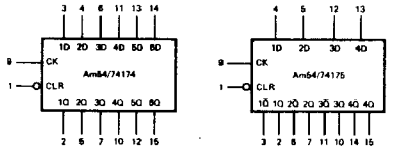
FUNCTIONAL DESCRIPTION

The Am54/74174 is a hex positive-edge-triggered D-type parallel register. The Am54/74175 is a quad positive-edge-triggered D-type parallel register with both Q and $\bar{Q}$ outputs available. Both registers feature a single common clock line and a single common clear line.

When the clear input is LOW, the Q outputs are LOW regardless of the other inputs. When the clear input is HIGH, the clock will transfer data on the D_i inputs to the Q_i outputs on the LOW-to-HIGH transition of the clock. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge. When the clock is at either a HIGH or a LOW, the D_i inputs have no effect on the Q_i outputs.

LOGIC SYMBOLS

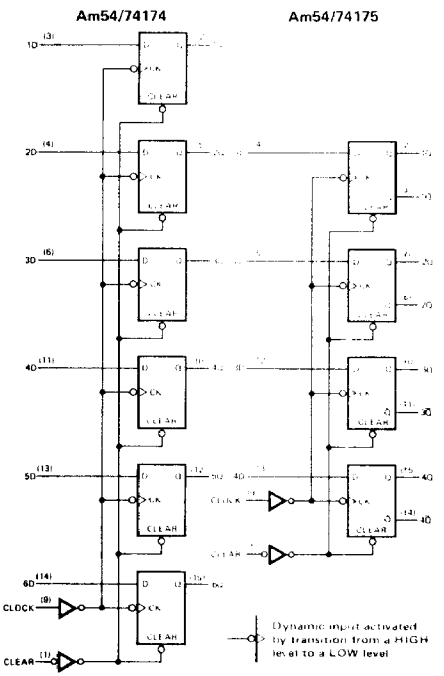
Am54/74174 Am54/74175



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL BLOCK DIAGRAMS

Am54/74174 Am54/74175

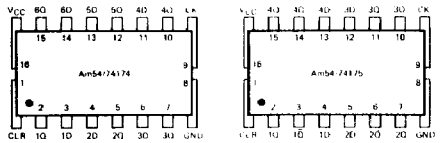


Am54/74174, Am54/74175 ORDERING INFORMATION

Package Type	Temperature Range	Am54/74174 Order Number	Am54/74175 Order Number
Molded DIP	0°C to 70°C	SN74174N	SN74175N
Hermetic DIP	0°C to 70°C	SN74174J	SN74175J
Dice	0°C to 70°C	SN74174X	SN74175X
Hermetic DIP	−55°C to +125°C	SN54174J	SN54175J
Hermetic Flat Pack	−55°C to +125°C	SN54174W	SN54175W
Dice	−55°C to +125°C	SN54174X	SN54175X

CONNECTION DIAGRAMS
Top View

Am54/74174 Am54/74175



MAXI RATINGS (Above which the useful life may be impaired)

Storage ,perature	−65°C to +150
Temperature (Ambient) Under Bias	−55°C to +125
Supply Voltage to Ground Potential Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5
Output Current, Into Outputs	30 m
DC Input Current	−30 mA to +5.0 m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74174, Am74175 T_A = 0°C to 70°C V_{CC} = 5.0 V ±5% (COM) MIN. = 4.75 V MAX. = 5.25 V
Am54174, Am54175 T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8mA V_{IN} = V_{IH} or V_{IL}		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4				−1.6	mA
I_{IH} (Note 3	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V				40	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.	54174, 5	−20		−57	mA
			74174, 5	−18		−57	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	54/74174		45	65	mA
			54/74175		30	45	

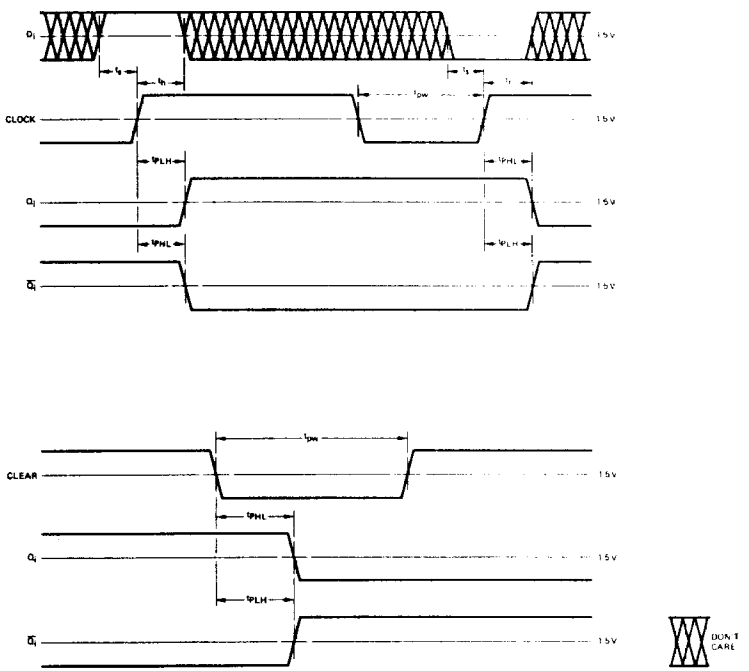
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input current = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. All outputs open. Data and clear inputs at 4.5 V. Measured after a momentary ground, then 4.5 V applied to the clock.

Switching Characteristics (T_A = 25°C)

Parameters	Description		Test Conditions	Limits Min.	Typ.	Max.	Units
$f_{max.}$	Maximum Clock Frequency		V_{CC} = 5.0V C_L = 15pF, R_L = 400Ω (See Switching Waveforms)	25	35		MHz
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output from Clear (Am54/74175 Only)				16	25	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output from Clear				23	35	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output from Clock				20	30	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output from Clock				21	30	ns
t_{pw}	Pulse Width	Clock		20			ns
		Clear		20			
t_s	Set-up Time	Data		20			ns
		Clear		25			
t_h	Hold Time - Data			5			ns

SWITCHING WAVEFORMS

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



DEFINITION OF TERMS

SUBSCRIPT TERMS

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS

D Information on the D input is written into the flip-flop on the positive going clock transition.

Q, $\overline{Q}$ The flip-flop outputs.

CK Clock. The clock input is common to all flip-flops and transfers data on the D input to the Q output on its LOW-to-HIGH transition.

CLR Clear. The clear input is common to all flip-flops. A LOW input sets the Q outputs to a LOW.

OPERATIONAL TERMS

I_L Forward input load current for unit input load.

I_{OH} Output HIGH current forced out of output in V_{OH} test.

I_{OL} Output LOW current forced into the output in V_{OL} test.

I_H Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the logic level)

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{pw} The minimum time between the 1.5V points on the leading and trailing edges of a pulse.

t_s Set-up-time. The time interval for which a signal must be applied and maintained at a specified level for a specified input terminal before an active transition occurs at another specified input terminal.

t_h Hold time. The time interval for which a signal is retained at a specified level for a specified input terminal after an active transition occurs at another specified input terminal.

FUNCTION TABLE
(Each Flip-Flop)

INPUTS			OUTPUTS	
Clear	Clock	D	Q	$\bar{Q}_1$
L	X	X	L	H
H	↓	H	H	L
H	↓	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

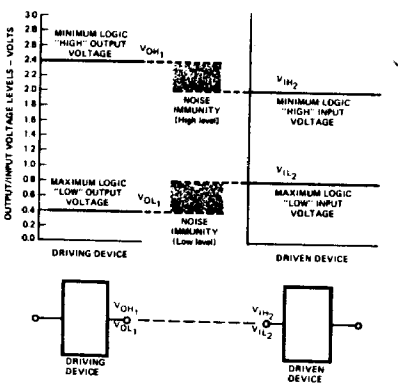
H = HIGH Level (Steady State)
L = LOW Level (Steady State)
X = Irrelevant
↓ = Transition from Low-to-High Level
Q_0 = The Level of Q before the Indicated Steady-State Input Conditions were Established.
† = Am54/74175 Only.

MSI INTERFACING RULES

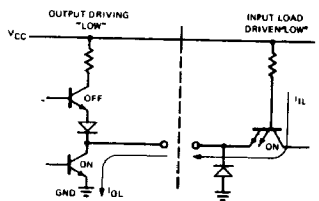
Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

INPUT/OUTPUT INTERFACE CONDITIONS

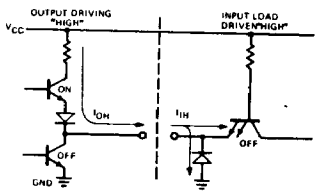
Voltage Interface Conditions – LOW & HIGH



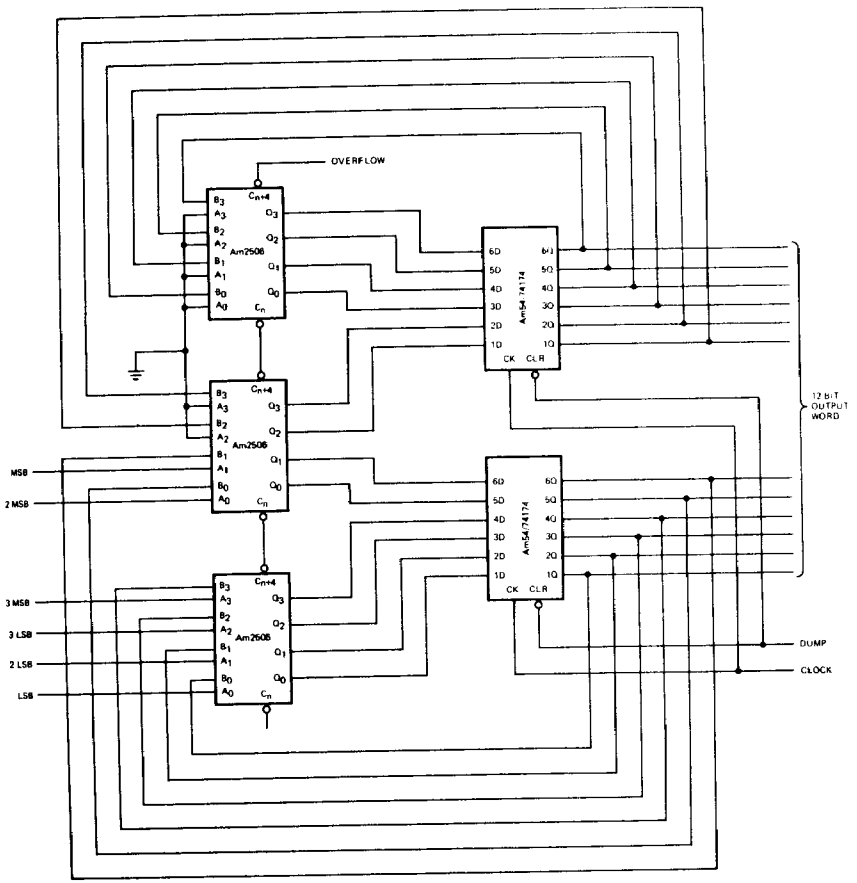
Current Interface Conditions – LOW



Current Interface Conditions – HIGH



APPLICATION



(Am2506 E = S_0 = HIGH; M = S_1 = S_2 = S_3 = LOW)

6-Bit Input, Integrate and Dump for Magnitude-Only Arithmetic (65 samples min. before overflow)

Am54/. . ./4 LOADING RULES (In Unit Loads)

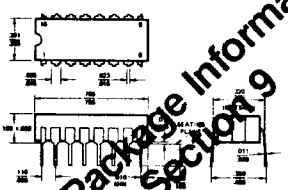
Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
Clear	1	1	–	–
1Q	2	–	20	10
1D	3	1	–	–
2D	4	1	–	–
2Q	5	–	20	10
3D	6	1	–	–
3Q	7	–	20	10
GND	8	–	–	–
CK	9	1	–	–
4Q	10	–	20	10
4D	11	1	–	–
5Q	12	–	20	10
5D	13	1	–	–
6D	14	1	–	–
6Q	15	–	20	10
V_{CC}	16	–	–	–

Am54/74175 LOADING RULES (In Unit Loads)

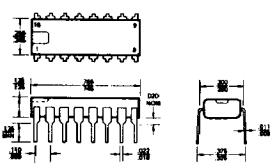
Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
Clear	1	1	–	–
1Q	2	–	20	10
$1\overline{Q}$	3	–	20	10
1D	4	1	–	–
2D	5	1	–	–
$2\overline{Q}$	6	–	20	10
2Q	7	–	20	10
GND	8	–	–	–
CK	9	1	–	–
3Q	10	–	20	10
$3\overline{Q}$	11	–	20	10
3D	12	1	–	–
4D	13	1	–	–
$4\overline{Q}$	14	–	20	10
4Q	15	–	20	10
V_{CC}	16	–	–	–

PHYSICAL DIMENSIONS
Dual-In-Line

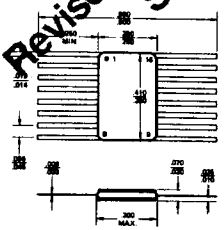
Ceramic



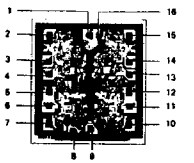
Molded



Flat Package



Metallization and Pad Layout



DIE SIZE .075" x .082"

ADVANCED MICRO DEVICES INC
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

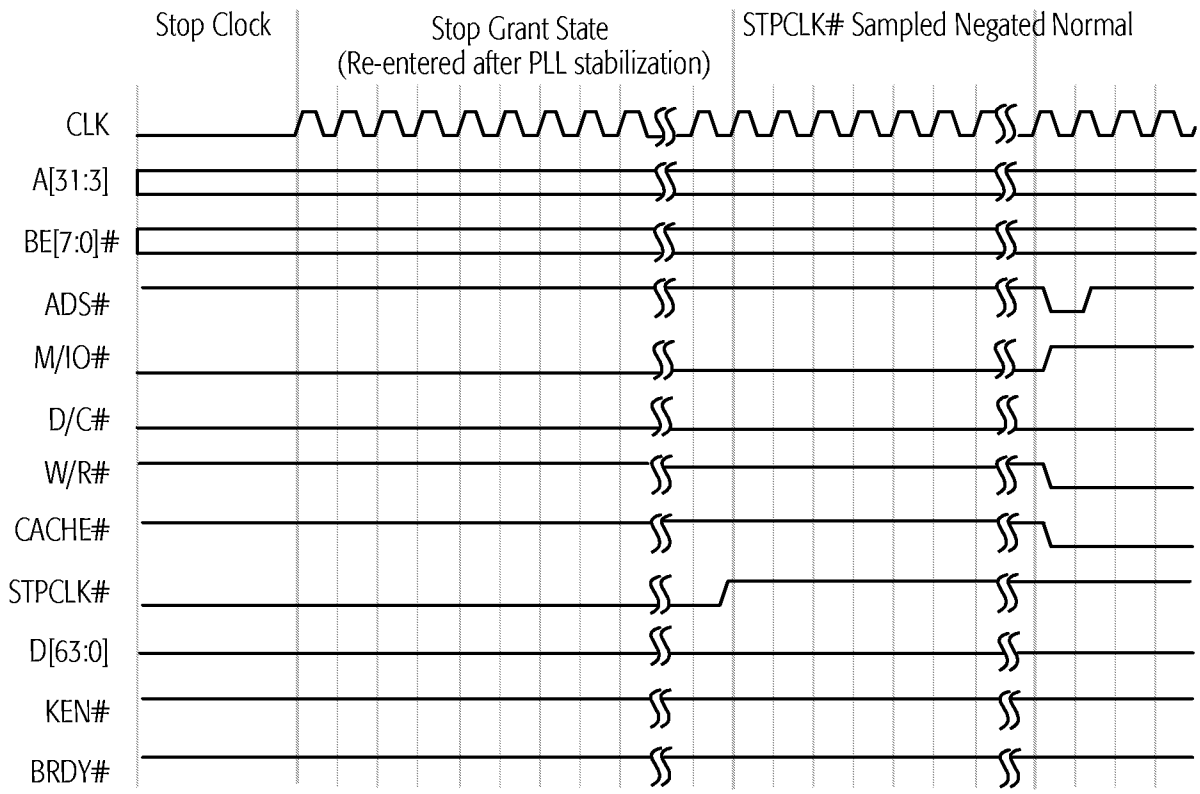


Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

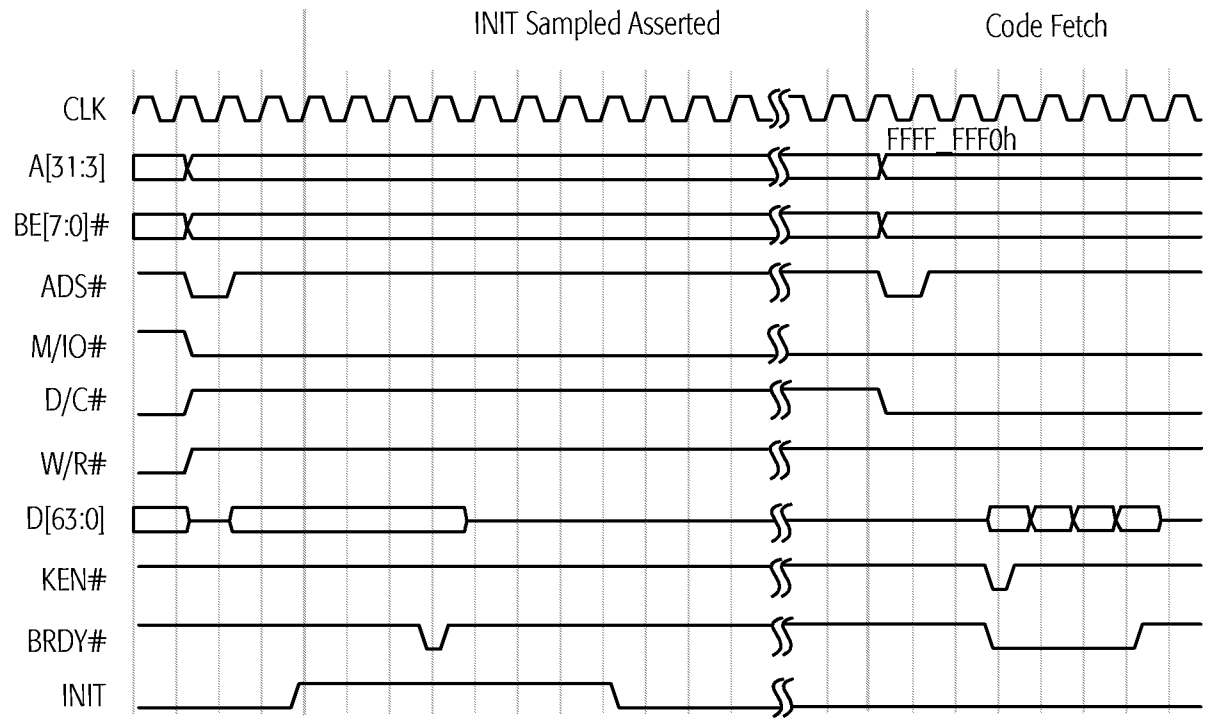


Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.