# Quad buffer (3-State) 74ABT126

## FEATURES

- Quad bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up 3-State
- Inputs are disabled during 3-State mode

## DESCRIPTION

The 74ABT126 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT126 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables (OE0, OE1, OE2, OE3), each controlling one of the 3-State outputs.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb}$ = 25°C; GND = 0V | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Propagation delay An to Yn | $C_L$ = 50pF; $V_{CC}$ = 5V | 2.9 | ns |
| $C_{IN}$ | Input capacitance | $V_I$ = 0V or $V_{CC}$ | 4 | pF |
| $C_{OUT}$ | Output capacitance | Outputs disabled; $V_O$ = 0V or $V_{CC}$ | 7 | pF |
| $I_{CCZ}$ | Total supply current | Outputs disabled; $V_{CC}$ = 5.5V | 65 | µA |

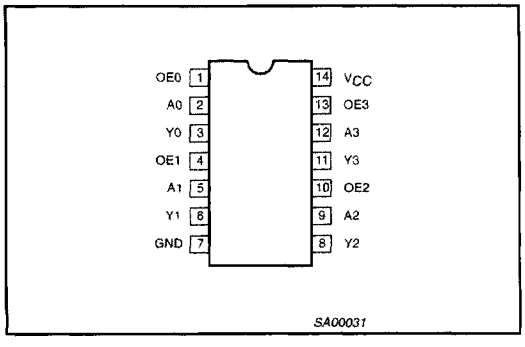
## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|---|---|---|---|---|
| 14-Pin Plastic DIP | –40°C to +85°C | 74ABT126 N | 74ABT126 N | SOT27-1 |
| 14-Pin plastic SO | –40°C to +85°C | 74ABT126 D | 74ABT126 D | SOT108-1 |
| 14-Pin Plastic SSOP Type II | –40°C to +85°C | 74ABT126 DB | 74ABT126 DB | SOT337-1 |
| 14-Pin Plastic TSSOP Type I | –40°C to +85°C | 74ABT126 PW | 74ABT126PW DH | SOT402-1 |

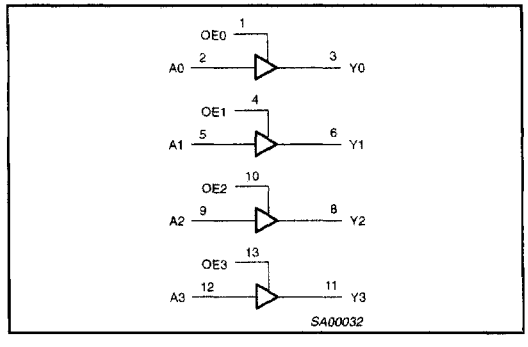
## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 2, 5, 9, 12 | A0 – A3 | Data inputs |
| 3, 6, 8, 11 | Y0 – Y3 | Data outputs |
| 1, 4, 10, 13 | OE0 – OE3 | Output enable inputs |
| 7 | GND | Ground (0V) |
| 14 | $V_{CC}$ | Positive supply voltage |

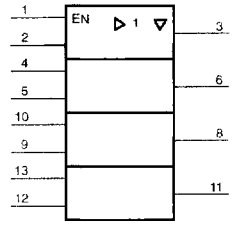
## PIN CONFIGURATION




## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)




## FUNCTION TABLE

| INPUTS | | OUTPUTS |
|---|---|---|
| OEn | An | Yn |
| H | L | L |
| H | H | H |
| L | X | Z |

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

## ABSOLUTE MAXIMUM RATINGS[1, 2]

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | −0.5 to +7.0 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | −18 | mA |
| $V_I$ | DC input voltage[3] | | −1.2 to +7.0 | V |
| $I_{OK}$ | DC output diode current | $V_O < 0$ | −50 | mA |
| $V_{OUT}$ | DC output voltage[3] | output in Off or High state | −0.5 to +5.5 | V |
| $I_{OUT}$ | DC output current | output in Low state | 128 | mA |
| $T_{stg}$ | Storage temperature range | | −65 to 150 | °C |

**NOTES:**
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | DC supply voltage | 4.5 | 5.5 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | 2.0 | | V |
| $V_{IL}$ | Low-level Input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | −32 | mA |
| $I_{OL}$ | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 10 | ns/V |
| $T_{amb}$ | Operating free-air temperature range | −40 | +85 | °C |

## DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C | | | $T_{amb}$ = –40°C to +85°C | | |
| | | | Min | Typ | Max | Min | Max | |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.5V; $I_{IK}$ = –18mA | | –0.9 | –1.2 | | –1.2 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = 4.5V; $I_{OH}$ = –3mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | 2.5 | 2.9 | | 2.5 | | V |
| | | $V_{CC}$ = 5.0V; $I_{OH}$ = –3mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | 3.0 | 3.4 | | 3.0 | | V |
| | | $V_{CC}$ = 4.5V; $I_{OH}$ = –32mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | 2.0 | 2.4 | | 2.0 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.5V; $I_{OL}$ = 64mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | | 0.35 | 0.55 | | 0.55 | V |
| $I_I$ | Input leakage current | $V_{CC}$ = 5.5V; $V_I$ = GND or 5.5V | | ±0.01 | ±1.0 | | ±1.0 | µA |
| $I_{OFF}$ | Power-off leakage current | $V_{CC}$ = 0.0V; $V_O$ or $V_I \leq$ 4.5V | | ±5.0 | ±100 | | ±100 | µA |
| $I_{PU}/I_{PD}$ | Power-up/down 3-State output current[3] | $V_{CC}$ = 2.1V; $V_O$ = 0.5V; $V_I$ GND or $V_{CC}$; $V_{OE}$ = Don't care | | ±5.0 | ±50 | | ±50 | µA |
| $I_{OZH}$ | 3-State output High current | $V_{CC}$ = 5.5V; $V_O$ = 2.7V; $V_I$ = $V_{IL}$ or $V_{IH}$ | | 1.0 | 50 | | 50 | µA |
| $I_{OZL}$ | 3-State output Low current | $V_{CC}$ = 5.5V; $V_O$ = 0.5V; $V_I$ = $V_{IL}$ or $V_{IH}$ | | –1.0 | –50 | | –50 | µA |
| $I_{CEX}$ | Output High leakage current | $V_{CC}$ = 5.5V; $V_O$ = 5.5V; $V_I$ = GND or $V_{CC}$ | | 5.0 | 50 | | 50 | µA |
| $I_O$ | Output current[1] | $V_{CC}$ = 5.5V; $V_O$ = 2.5V | –50 | –100 | –180 | –50 | –180 | mA |
| $I_{CCH}$ | Quiescent supply current | $V_{CC}$ = 5.5V; Outputs High, $V_I$ = GND or $V_{CC}$ | | 65 | 250 | | 250 | µA |
| $I_{CCL}$ | | $V_{CC}$ = 5.5V; Outputs Low, $V_I$ = GND or $V_{CC}$ | | 12 | 15 | | 15 | mA |
| $I_{CCZ}$ | | $V_{CC}$ = 5.5V; Outputs 3–State; $V_I$ = GND or $V_{CC}$ | | 65 | 250 | | 250 | µA |
| $\Delta I_{CC}$ | Additional supply current per input pin[2] | Outputs enabled, one data input at 3.4V, other inputs at $V_{CC}$ or GND; $V_{CC}$ = 5.5V | | 0.5 | 1.5 | | 1.5 | mA |
| | | Outputs 3-State, one data input at 3.4V, other inputs at $V_{CC}$ or GND; $V_{CC}$ = 5.5V | | 50 | 250 | | 250 | µA |
| | | Outputs 3-State, one enable input at 3.4V, other inputs at $V_{CC}$ or GND; $V_{CC}$ = 5.5V | | 0.5 | 1.5 | | 1.5 | mA |

**NOTES:**
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any $V_{CC}$ between 0V and 2.1V, with a transition time of up to10msec. From $V_{CC}$ = 2.1V to $V_{CC}$ = 5V ± 10%, a transition time of up to 100µsec is permitted.

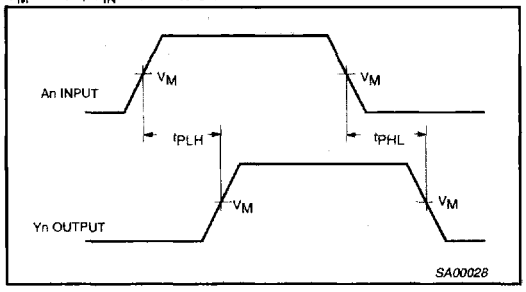
## AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; $C_L$ = 50pF, $R_L$ = 500Ω

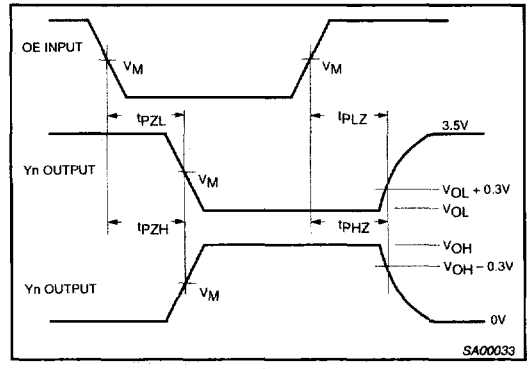
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C $V_{CC}$ = +5.0V | | | $T_{amb}$ = –40°C to +85°C $V_{CC}$ = +5.0V ±0.5V | | |
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>An to Yn | 1 | 1.0<br>1.0 | 2.9<br>3.0 | 4.2<br>4.3 | 1.0<br>1.0 | 4.4<br>4.6 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time<br>to High and Low level | 2 | 1.9<br>1.9 | 3.2<br>4.4 | 5.8<br>5.9 | 1.9<br>1.9 | 6.5<br>6.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time<br>from High and Low level | 2 | 1.0<br>1.0 | 4.2<br>2.9 | 5.2<br>4.9 | 1.0<br>1.0 | 5.8<br>5.5 | ns |

## AC WAVEFORMS

$V_M$ = 1.5V, $V_{IN}$ = GND to 3.0V

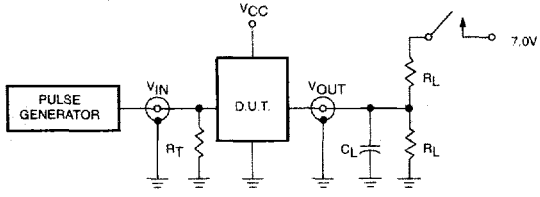



**Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays**

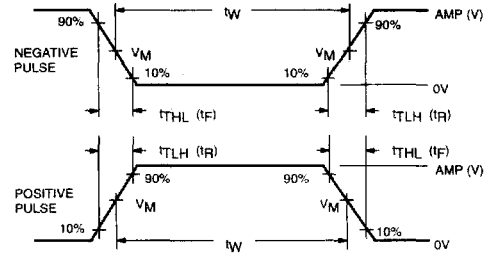



**Waveform 2. Waveforms Showing the 3–State Output Enable and Disable Times**

## TEST CIRCUIT AND WAVEFORMS




**Test Circuit for 3-State Outputs**




$V_M$ = 1.5V

**Input Pulse Definition**

### SWITCH POSITION

| TEST | SWITCH |
|---|---|
| $t_{PLZ}$ | closed |
| $t_{PZL}$ | closed |
| All other | open |

### DEFINITIONS

$R_L$ = Load resistor; see AC CHARACTERISTICS for value.

$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|---|---|---|---|---|---|
| | Amplitude | Rep. Rate | $t_W$ | $t_R$ | $t_F$ |
| 74ABT | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

SA00012