HARRIS SEMICONDUCTOR

CD74LCX16373

January 1998

Fast CMOS 3.3V 16-Bit Transparent Latch

Features

- **Advanced 0.6 micron CMOS Technology**
- **5V Tolerant Inputs and Outputs**
- **Supports Live Insertion of PCBs**
- **2.0V to 3.6V V_{CC} Supply Range**
- **Balanced 24mA Output Drive**
- **Low Ground Bounce Outputs**
- **ESD Protection Exceeds 2000V, HBM; 200V, MM**
- **Functionally Compatible with FCT3, LVC, LVT, and 74 Series Logic Families**

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CD74LCX16373MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LCX16373SM	-40 to 85	48 Ld SSOP	M48.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

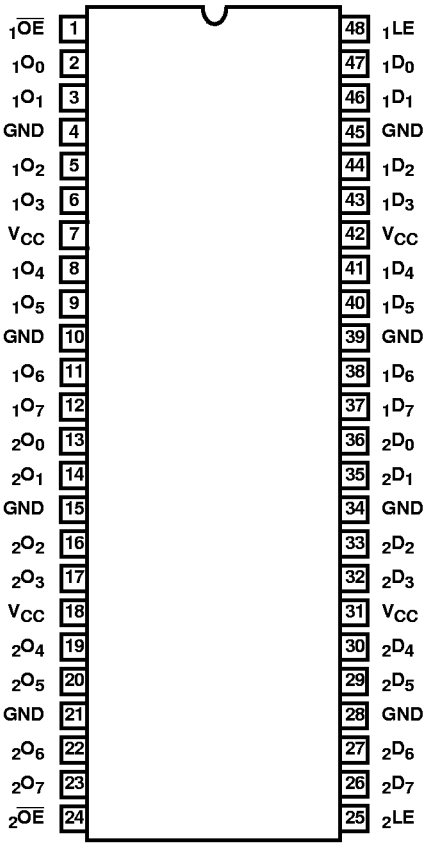
Description

The CD74LCX16373 is a 16-bit transparent latch designed with three-state outputs and is intended for bus oriented applications. The Output Enable and Latch Enable controls are organized to operate as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

The CD74LCX16373 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

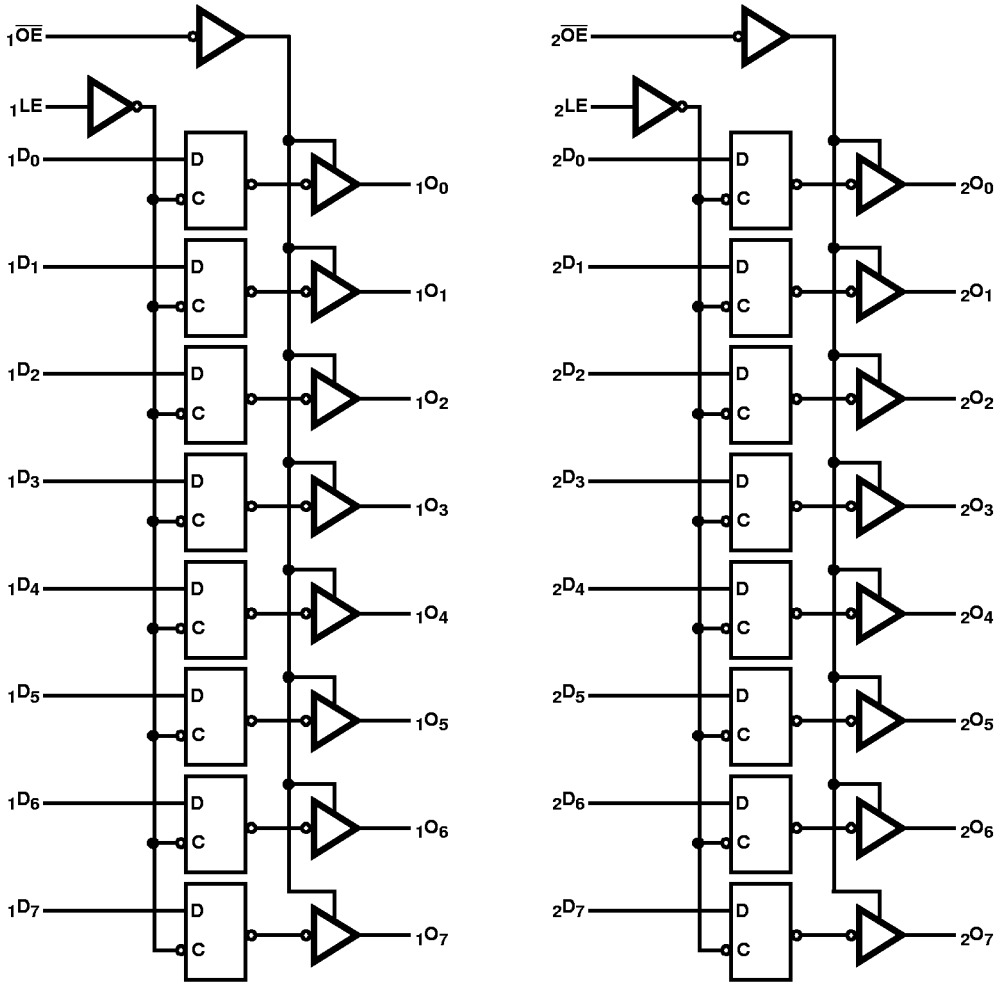
CD74LCX16373
(SSOP, TSSOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4435**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$_XD_X$	$_X\overline{OE}$	$_XLE$	$_XO_X$
H	L	H	H
L	L	H	L
X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_X\overline{OE}$	Output Enable Inputs (Active LOW)
$_XLE$	Latch Enable Inputs (Active HIGH)
$_XD_X$	Data Inputs
$_XO_X$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40^oC to 85^oC
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Operating . . . . . 2.0V to 3.6V
Data Retention . . . . . 1.5V to 3.6V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^oC$ to 85^oC, $V_{CC} = 2.7V$ to $3.6V$							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Output HIGH Voltage	V_{OH}	$V_{CC} = 2.7V$ to $3.6V$	$I_{OH} = -0.1mA$	$V_{CC} - 0.2$	-	-	V
		$V_{CC} = 2.7V$	$I_{OH} = -12mA$	2.2	-	-	V
		$V_{CC} = 3.0V$	$I_{OH} = -18mA$	2.4	-	-	V
			$I_{OH} = -24mA$	2.2	-	-	V
Output LOW Voltage	V_{OL}	$V_{CC} = 2.7V$ to $3.6V$	$I_{OL} = 0.1mA$	-	-	0.2	V
		$V_{CC} = 2.7V$	$I_{OL} = 12mA$	-	-	0.4	V
		$V_{CC} = 3V$	$I_{OL} = 16mA$	-	-	0.4	V
			$I_{OL} = 24mA$	-	-	0.55	V
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, $I_{IN} = -18mA$		-	-0.7	-1.2	V
Input Current	I_I	$V_{CC} = 2.7V$ to $3.6V$	$0 \le V_I \le 5.5V$	-	-	±5	µA
High Impedance Output Current (Three-State)	I_{OZ}	$V_{CC} = 2.7V$ to $3.6V$	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	-	-	±5	µA
Power Down Disable	I_{OFF}	$V_{CC} = 0V$	V_{IN} or $V_{OUT} \le 5.5V$	-	-	10	µA
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC} - 0.6V$ (Note 5)	-	-	500	µA
CAPACITANCE							
Input Capacitance (Note 6)	C_{IN}	V_{CC} = Open, $V_{IN} = 0V$ or V_{CC}		-	7	-	pF

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS	MIN	(NOTE 4) TYP	MAX	UNITS
Output Capacitance (Note 6)	C_{OUT}	V_{CC} = 3.3V, V_{IN} = 0V or V_{CC}	-	8	-	pF
Power Dissipation Capacitance (Note 7)	C_{PD}	V_{CC} = 3.3V, V_{IN} = 0V or V_{CC}, f = 10MHz	-	25	-	pF

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Per TTL driven input; all other inputs at V_{CC} or GND.
6. This parameter is determined by device characterization but is not production tested.
7. C_{PD} determines the no-load dynamic power consumption per latch. It is obtained by the following relationship: P_D (total power per latch) = V_{CC}^2 f_i (C_{PD} + C_L) where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply range.

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 8) TEST CONDITIONS	V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V		UNITS
			(NOTE 9) MIN	MAX	(NOTE 9) MIN	MAX	
Propagation Delay D_n to O_n	t_{PLH}, t_{PHL}	C_L = 50 pF, R_L = 500Ω	1.5	5.4	1.5	5.9	ns
Propagation Delay LE to O_n	t_{PLH}, t_{PHL}		1.5	5.5	1.5	6.4	ns
Output Enable Time	t_{PZH}, t_{PZL}		1.5	6.1	1.5	6.5	ns
Output Disable Time (Note 10)	t_{PHZ}, t_{PLZ}		1.5	6.0	1.5	6.3	ns
Setup Time, D_n to LE	t_S		2.5	-	2.5	-	ns
Hold Time, D_n to LE	t_H		1.5	-	1.5	-	ns
LE Pulse Width, (Note 10)	t_W		3.0	-	3.0	-	ns
Output Skew, (Note 11)	$t_{SK(O)}$		-	1.0	-	-	ns

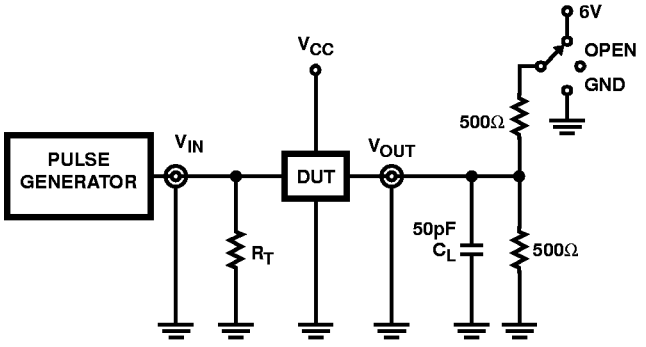
NOTES:

8. See test circuit and waveforms.
9. Minimum limits are guaranteed but not tested on Propagation Delays.
10. This parameter is guaranteed but not production tested.
11. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
12. Measured with n-1 outputs switching from High-to-Low or Low-to-High. The remaining output is measured in the LOW state.

Dynamic Switching Characteristics T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS (NOTE 12)	TYP	UNITS
Dynamic LOW Peak Voltage	V_{OLP}	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	0.8	V
Dynamic LOW Valley Voltage	V_{OLV}	V_{CC} = 3.3V, C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	0.8	V

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

13. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

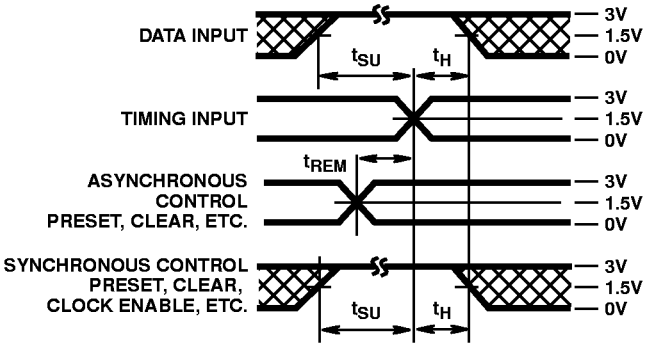


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

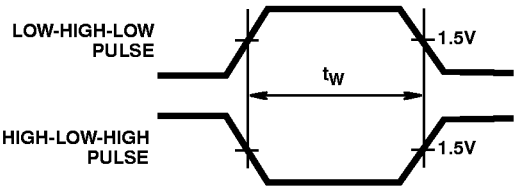


FIGURE 3. PULSE WIDTH

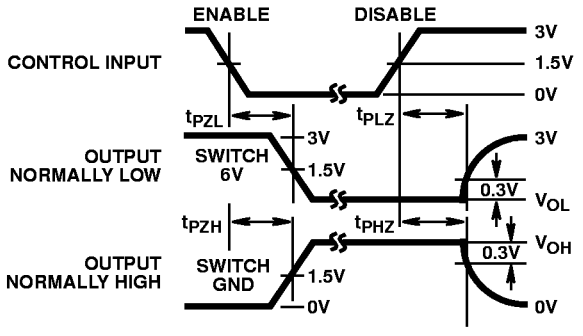


FIGURE 4. ENABLE AND DISABLE TIMING

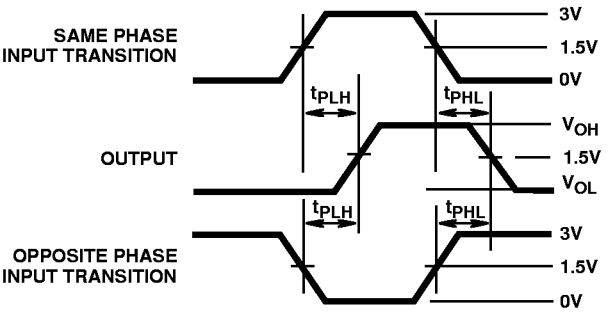
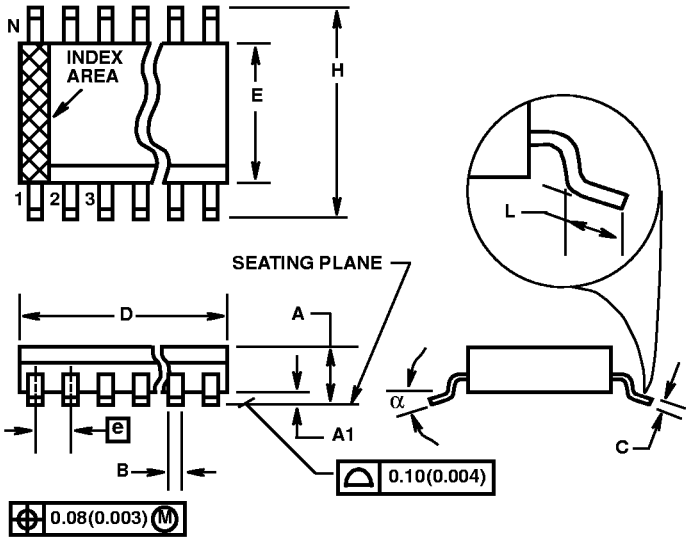


FIGURE 5. PROPAGATION DELAY

Thin Shrink Small Outline Plastic Packages (TSSOP)



M48.240-P

48 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.041	0.047	1.05	1.20	-
A1	0.002	0.006	0.05	0.15	-
B	0.007	0.010	0.178	0.254	-
C	0.004	0.008	0.102	0.203	-
D	0.488	0.496	12.40	12.59	1
E	0.236	0.244	6.00	6.19	2
e	0.0197 BSC		0.50 BSC		-
H	0.307	0.330	7.80	8.38	-
L	0.020	0.030	0.51	0.76	3
N	48		48		4
α	0^o	8^o	0^o	8^o	-

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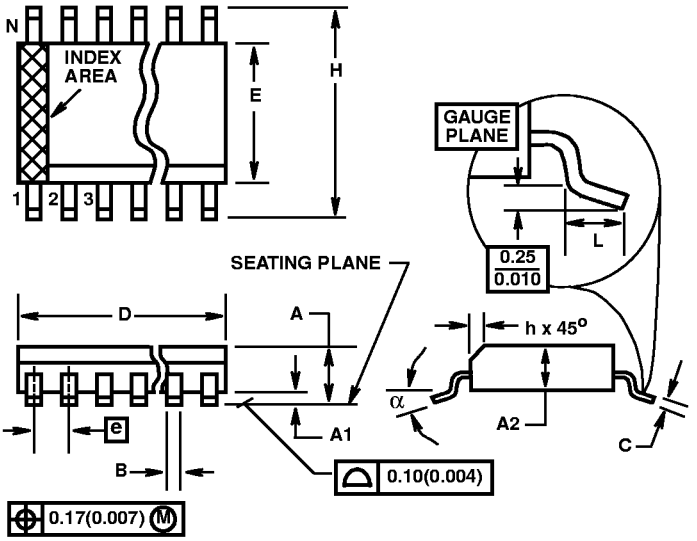
NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs.
2. Dimension “E” does not include interlead flash or protrusions.
3. “L” is the length of terminal for soldering to a substrate.
4. “N” is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



M48.300-P

48 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.096	0.108	2.44	2.74	-
A1	0.008	0.016	0.20	0.41	-
A2	0.088	0.092	2.24	2.34	-
B	0.008	0.0135	0.20	0.34	-
C	0.005	0.010	0.13	0.25	-
D	0.620	0.630	15.75	16.00	2
E	0.291	0.299	7.39	7.59	3
e	0.025 BSC		0.635 BSC		-
H	0.395	0.415	10.03	10.54	-
h	0.015	0.025	0.381	0.635	-
L	0.020	0.040	0.51	1.01	4
N	48		48		5
α	0^o	8^o	0^o	8^o	-

Rev. 0 5/96

NOTES:

1. These package dimensions are within allowable dimensions of JECEC MO-118-AA, Issue B.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
3. Dimension “E” does not include interlead flash or protrusions.
4. “L” is the length of terminal for soldering to a substrate.
5. “N” is the number of terminal positions.
6. Terminal numbers are shown for reference only.
7. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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