NL27WZ07

Product Preview

Dual Buffer with Open Drain Outputs

The NL27WZ07 is a high performance dual buffer with open drain outputs operating from a 2.3 to 5.5 V supply.

The internal circuit is composed of multiple stages, including an open drain output which provides the capability to set output switching level. This allows the NL27WZ07 to be used to interface 5 V circuits to circuits of any voltage between V_{CC} and 7 V using an external resistor and power supply.

Current drive capability is 24 mA at the outputs.

- Extremely High Speed: t_{PD} 2.5 ns (typical) at V_{CC} = 5 V
- Designed for 2.3 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs
- LVTTL Compatible – Interface Capability With 5 V TTL Logic with V_{CC} = 3 V
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements

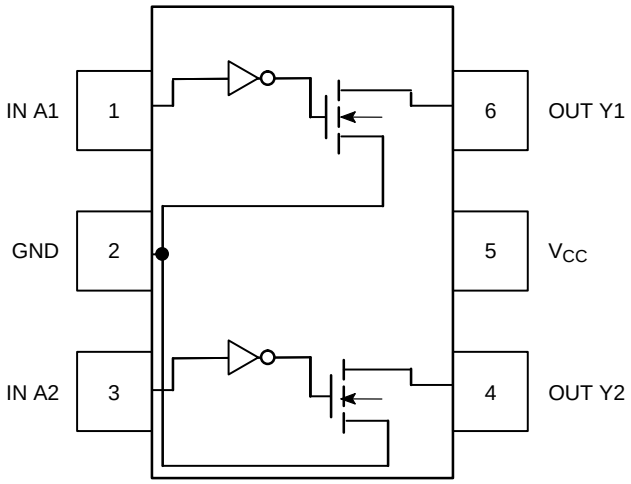

Figure 1. 6–Lead SOT–363 Pinout (Top View)

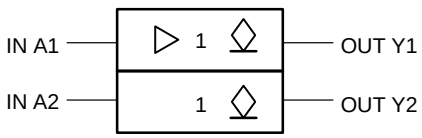

Figure 2. Logic Symbol

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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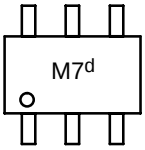
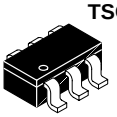
MARKING DIAGRAMS

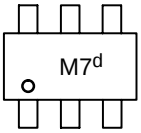
SC–88 / SOT–363/SC–70
DF SUFFIX
CASE 419B



Pin 1
d = Date Code



TSOP–6/SOT–23/SC–59
DT SUFFIX
CASE 318G



Pin 1
d = Date Code

PIN ASSIGNMENT

1	IN A1
2	GND
3	IN A2
4	OUT Y2
5	V_{CC}
6	OUT Y1

FUNCTION TABLE

A Input	Y Output
L	L
H	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition	Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +7.0	V
V_I	DC Input Voltage		$–0.5 \le V_I \le +7.0$	V
V_O	DC Output Voltage	Output in HIGH or LOW State.(Note 3.)	$–0.5 \le V_O \le V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	V_I < GND	–50	mA
I_{OK}	DC Output Diode Current	V_O < GND	–50	mA
		$V_O > V_{CC}$	+50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current Per Supply Pin		±100	mA
I_{GND}	DC Ground Current Per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		–65 to +150	°C
P_D	Power Dissipation in Still Air SC–88, TSOP–6	 per derating (Note 2.)	 200	mW
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 4.) Machine Model (Note 5.) Charged Device Model (Note 6.)	> 2000 > 200 > 3000	V
$I_{Latch–Up}$	Latch–Up Performance	Above V_{CC} and Below GND at 85°C (Note 7.)	±500	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.
2. Derating — SC–88 Package: –3 mW/°C from 65° to 125°C
   — TSOP–6 Package: –5 mW/°C from 65° to 125°C
3. I_O absolute maximum rating must be observed.
4. Tested to EIA/JESD22–A114–A
5. Tested to EIA/JESD22–A115–A
6. Tested to JESD22–C101–A
7. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.3 1.5	5.5 5.5	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	(HIGH or LOW State)	0	V_{CC}	V
I_{OH}	HIGH Level Output Current	V_{CC} = 4.5 V – 5.5 V V_{CC} = 3.0 V – 3.6 V V_{CC} = 2.7 V – 3.0 V V_{CC} = 2.3 V – 2.7 V		– 32 – 24 – 12 – 8	mA
I_{OL}	LOW Level Output Current	V_{CC} = 4.5 V – 5.5 V V_{CC} = 3.0 V – 3.6 V V_{CC} = 2.7 V – 3.0 V V_{CC} = 2.3 V – 2.7 V		+ 32 + 24 + 12 + 8	mA
T_A	Operating Free–Air Temperature		–40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 2.5 V ±0.2 V V_{CC} =3.0 V ±0.3 V V_{CC} =5.0 V ±0.5 V	0 0 0	20 10 5	ns/V

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

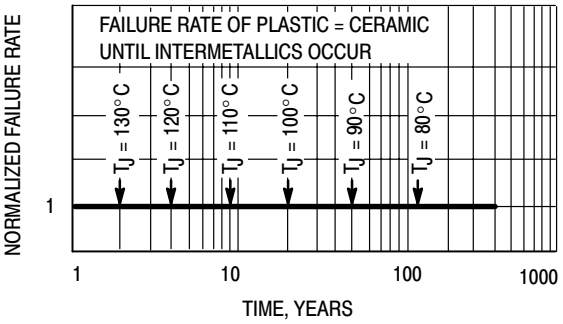


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			$T_A \le$ 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}		V
V_{IL}	Maximum Low–Level Input Voltage		2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}	V
I_{LKG}	Maximum Low–Level Output Leakage Current	V_{IN} = V_{IL} and V_{OUT} = V_{CC} or GND	2.3 to 5.5			±5.0		±10.0	μA
V_{OL}	Maximum Low–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.3 to 5.5			0.1		0.1	V
		I_{OL} = 8 mA	2.3		TBD	0.3		0.3	
		I_{OL} = 12 mA	2.7		TBD	0.4		0.4	
		I_{OL} = 16 mA	3.0		TBD	0.4		0.4	
		I_{OL} = 24 mA	3.0		TBD	0.55		0.55	
		I_{OL} = 32 mA	4.5		TBD	0.55		0.55	
I_{IN}	Maximum Input Leakage Current	V_{IN} or V_{OUT} = V_{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I_{OFF}	Maximum Off–State Leakage Current	V_{OUT} = 5.5 V	0			1		10	nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS $t_R = t_F$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			$T_A \le$ 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PZL}	Maximum Output Enable Time Input A to Y Figure 4. and 5.	R_L = R_1= 500 Ω, C_L = 50 pF	2.5 ± 0.2	1.2	3.7	5.8	1.2	6.4	ns
		R_L = R_1= 500 Ω, C_L = 50 pF	3.3 ± 0.3	0.8	2.9	4.4	0.8	4.8	
		R_L = R_1= 500 Ω, C_L = 50 pF	5.0 ± 0.5	0.5	2.3	3.5	0.5	3.9	
t_{PLZ}	Maximum Output Disable Time Input A to Y Figure 4. and 5.	R_L = R_1= 500 Ω, C_L = 50 pF	2.5 ± 0.2	1.2	2.8	5.8	1.2	6.4	ns
		R_L = R_1= 500 Ω, C_L = 50 pF	3.3 ± 0.3	0.8	2.1	4.4	0.8	4.8	
		R_L = R_1= 500 Ω, C_L = 50 pF	5.0 ± 0.5	0.5	1.4	3.5	0.5	3.9	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance (Note 8.)	10 MHz, V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	25	pF

8. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

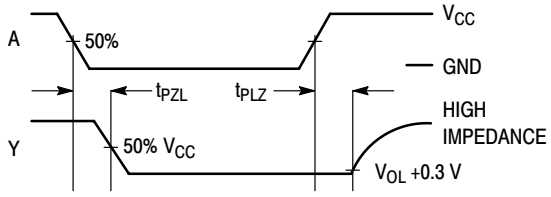
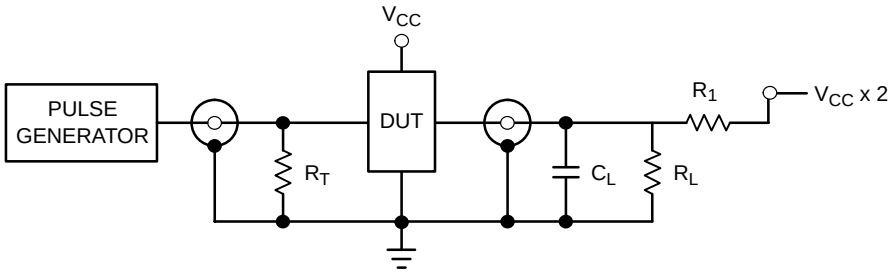


Figure 4. Switching Waveforms



R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 5. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NL27WZ07DFT2	NL	2	7	WZ	07	DF	T2	SC–88 / SOT–363 / SC–70	178 mm (7”) 3000 Unit
NL27WZ07DFT4	NL	2	7	WZ	07	DF	T4	SC–88 / SOT–363 / SC–70	330 mm (13”) 10000 Unit
NL27WZ07DTT1	NL	2	7	WZ	07	DT	T1	TSOP–6 / SOT–23 / SC–59	178 mm (7”) 3000 Unit
NL27WZ07DTT3	NL	2	7	WZ	07	DT	T3	TSOP–6 / SOT–23 / SC–59	330 mm (13”) 10000 Unit

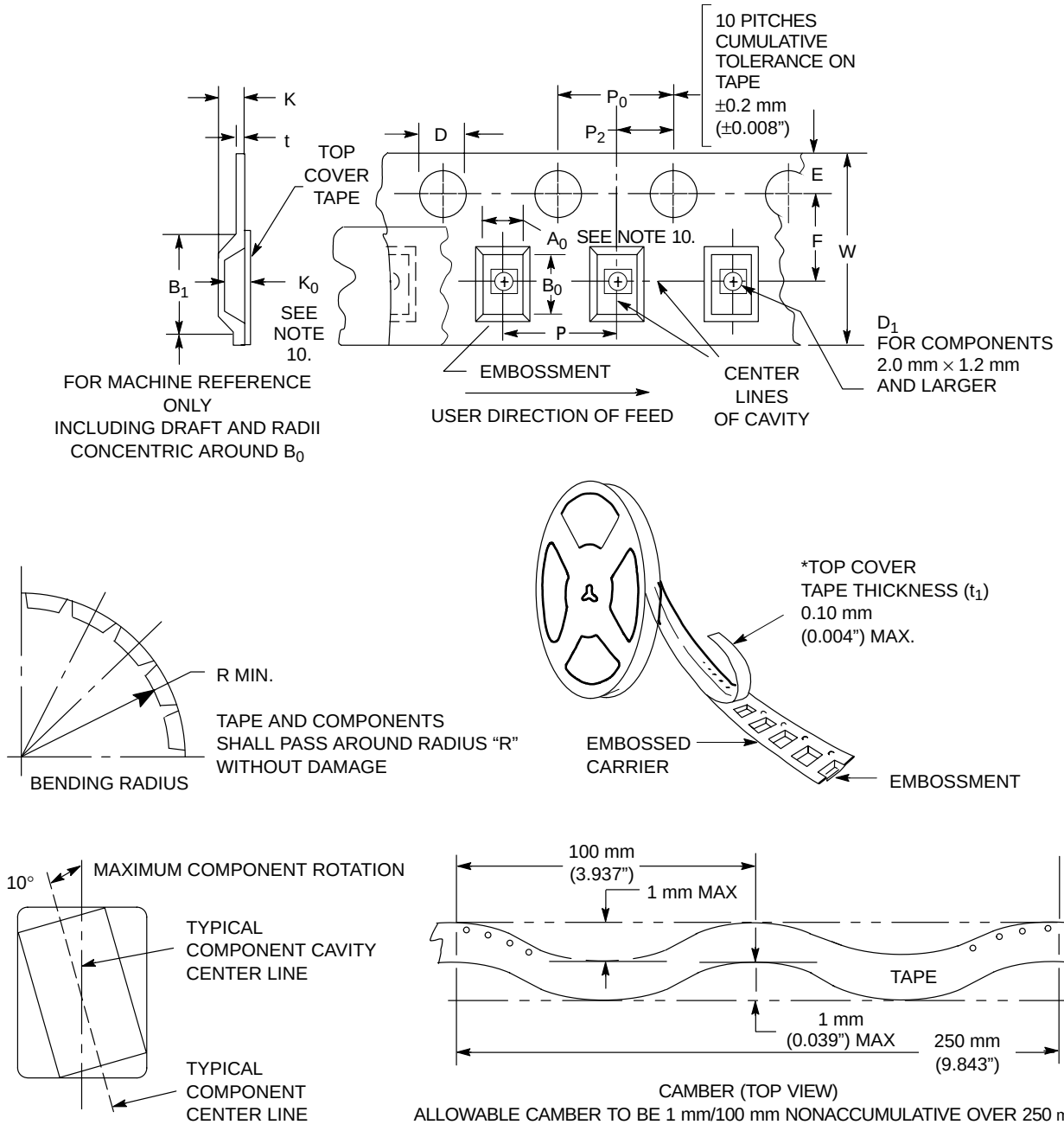


Figure 6. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 9. and 10.)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.35 mm (0.171")	1.5 +0.1/ –0.0 mm (0.059 +0.004/ –0.0")	1.0 mm Min (0.039")	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/ –0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

9. Metric Dimensions Govern–English are in parentheses for reference only.
10. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

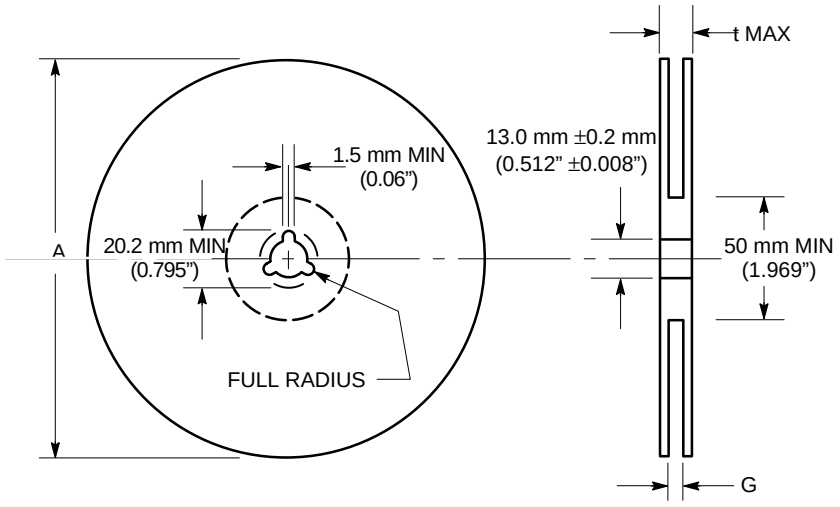


Figure 7. Reel Dimensions

REEL DIMENSIONS

Tape Size	T&R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7”)	8.4 mm, +1.5 mm, –0.0 (0.33” + 0.059”, –0.00)	14.4 mm (0.56”)
8 mm	T3, T4	330 mm (13”)	8.4 mm, +1.5 mm, –0.0 (0.33” + 0.059”, –0.00)	14.4 mm (0.56”)

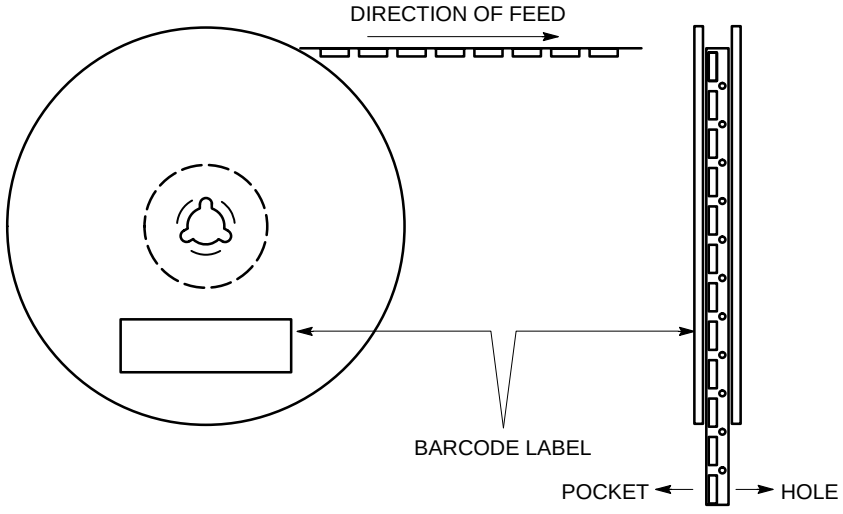


Figure 8. Reel Winding Direction

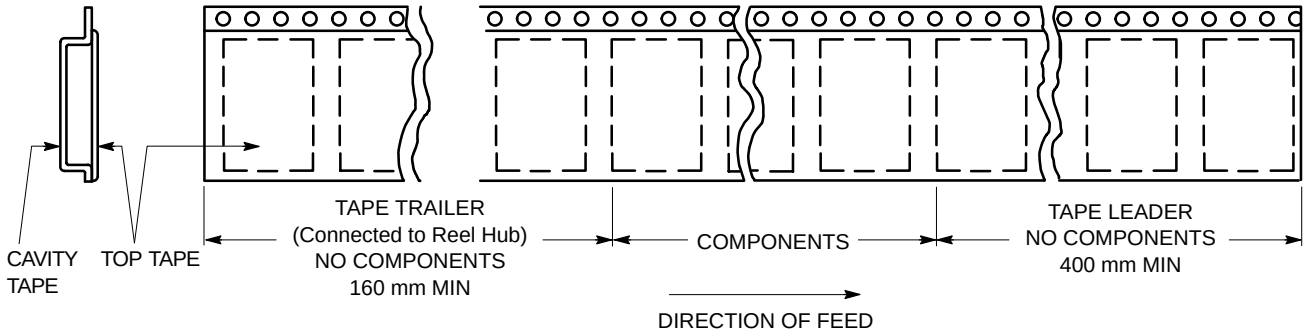


Figure 9. Tape Ends for Finished Goods

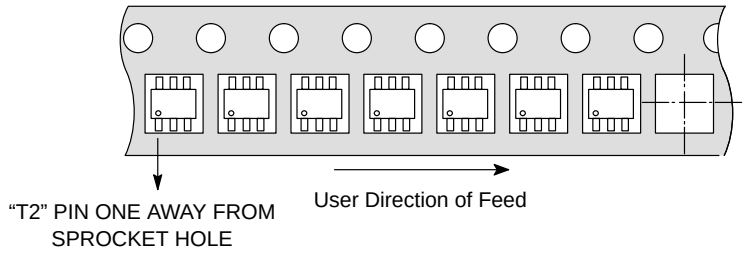


Figure 10. DFT2 and DFT4 (SC88) Reel Configuration/Orientation

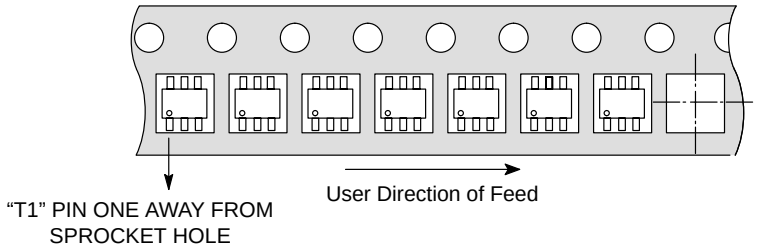
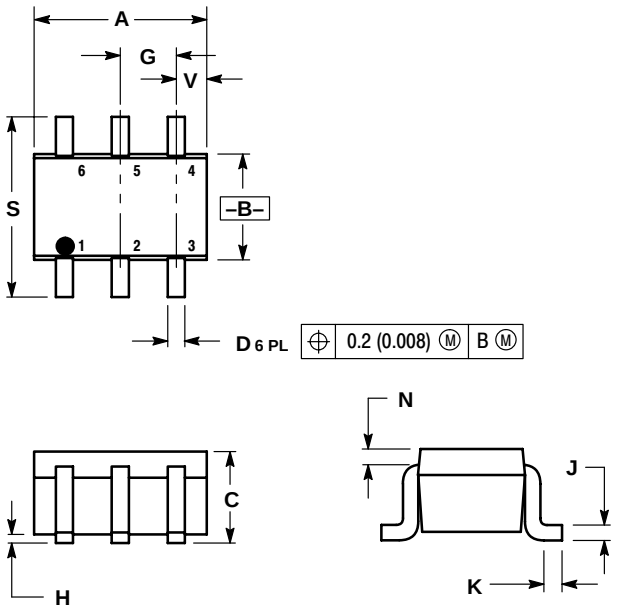


Figure 11. DTT1 and DTT3 (TSOP6) Reel Configuration/Orientation

PACKAGE DIMENSIONS

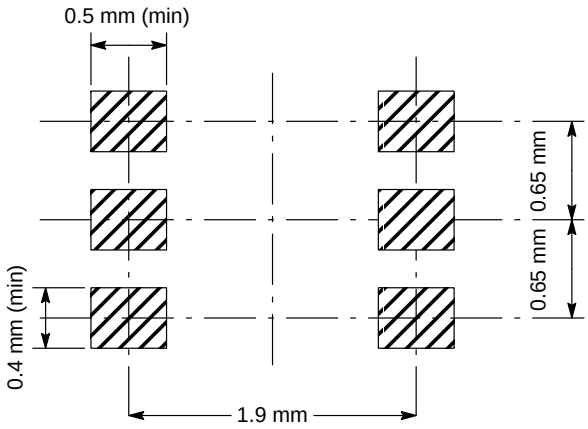
SC−88/SOT−363/SC−70
DF SUFFIX
CASE 419B−01
ISSUE G

SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

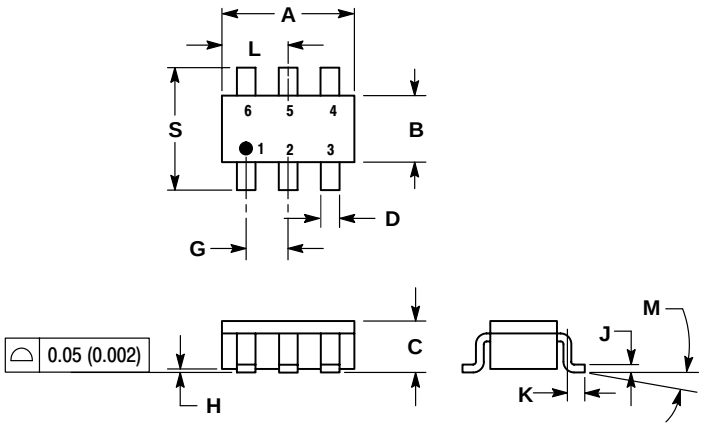
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40



PACKAGE DIMENSIONS

TSOP–6/SOT–23/SC–59
DT SUFFIX
CASE 318G–02
ISSUE G

SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

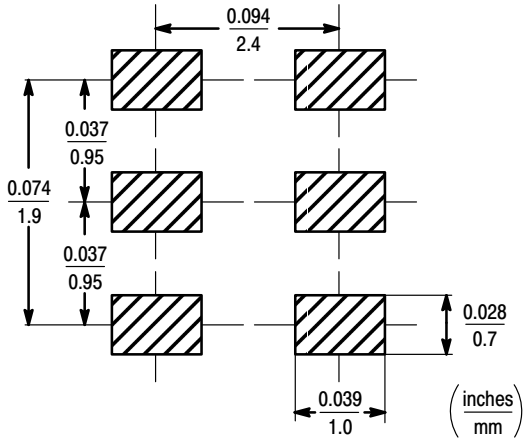
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD



Notes

Notes

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